S/M No. : DSD230FEF0

Service Manual

Digital Satellite Reciever

CHASSIS : SD-230

Model : DSD-9250E

Caution
: In this Manual, some parts can be changed for improving. their performance without notice in the parts list. So, if you need the latest parts information, please refer to PPL(Parts Price List)in Service Information Center(http://svc.dwe.co.kr)

DAEWOO ELECTRONICS

http : //svc.dwe.co.kr

Apr. 2003

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Ⅰ. GENERAL INFORMATION

1. GENERAL INFORMATION

A Digital Satellite Receiver is a convenient product that allows you to view a variety of programs provided through satellite. This user's guide covers the installation of the DSR and the necessary steps to implement various features. This also explains special features available only in this DSR in detail, which will allow you to make full of these feature.

2. Main Feature of DSD-9250E

- High quality Digital Video & Audio
- Fully MPEG2, DVB compliant
- One step direct move menu system (Go To function)
- Provide friendly and easy-to-use menu system
- Install Wizard system in the earliest of the world
- Various channel editing function
  (favorite, moving, locking, renaming, deleting and sorting)
- User programmable various Satellite & Transponder information
- Automatically search for newly added transponder
- Stores up to 2000 channels
- Easy and speedy software upgrade through RS-232 port
- Plug-and-plug data transfer system (DSR to DSR)
- Automatically each channel volume saving function
- Timer function, automatically turns On/Off by setting function
  (daily, weekly, monthly, one time)
- Automatic reserved channel moving system
- Provide Electronic Program Guide (EPG)
- Teletext function support
- Antenna Positioning Help feature
- Selectable Video output (CVBS, RGB, S-VHS)
- Provide various switch types, LNB types and NTSC/PAL monitor type
- SCPC/MCPC Receivable from C/Ku Band Satellite
- Multi LNB controlled by DiSEqC 1.0 DiSEqC 1.2 and 22KHz switching
- 256 colors On-Screen-Display
- PAL&NTSC Video Compatible (TV Type auto detect)
- Last channel auto saving

3. For Your Safety

- Allow clear space around the DSD-9250E for sufficient ventilation
- Do not cover the DSD-9250E or place it on a unit that emits heat
- Use a soft cloth and a mild solution of washing-up liquid to clean the casing
- Do not connect or modify cables when the DSD-9250E is plugged in.
- Do not remove the cover
- Do not allow the unit to be exposed to hot, cold or humid conditions
- Never allow liquids, spray or other materials to come into contact with the inside of the DSD-9250E

4. Unpacking

After purchasing the DSR, unpack it and check to make sure that all of the following items are included in the packaging

- 1 x Remote Control Unit (RCU)
- 1 x User's Guide
- 1 x DSR

5. General Operation of DSD-9250E

Throughout this manual you will notice that the everyday operation of your DSD-9250E is based on a series of user friendly on screen display and menus. These menus will help you get the most from your DSD-9250E, guiding you through installation, channel organizing, viewing and many other functions.

All function can be carried out using the buttons on the remote control, and some of the function can also be carried out using the buttons on the front panel.

If at any time when you using the menus you want to return to the normal TV mode, press the TV/AV button.

The DSD-9250E is easy to use, always at your command and adaptable for future advances.

Please be aware that new software may change the functionality of the DSD-9250E

Should you experience and difficulties with the operation of your DSD-9250E, please consult the relevant section of this manual, including the Problem Shooting, or alternatively call your dealer or a customer service adviser.

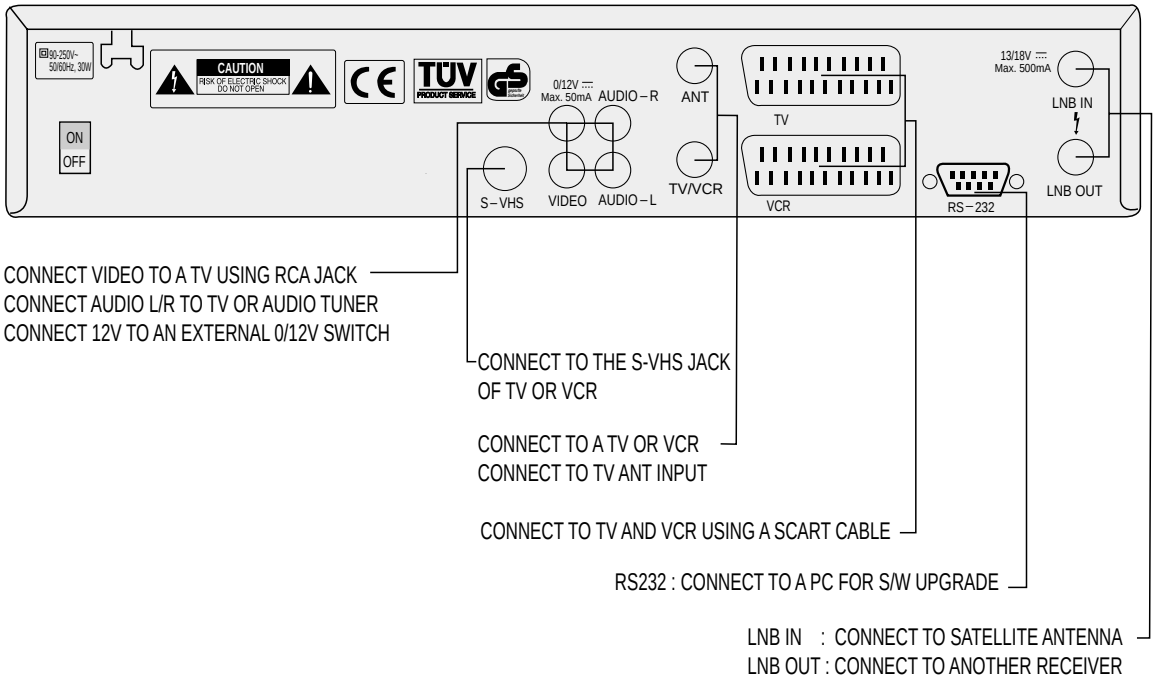
6. Remote Control

Key	Function
⏻	Switches between the operational mode and stand-by mode of the receiver (Green lamp lights up during the operation, Red lamp lights up in stand-by mode)
TV/ RADIO	Switches between TV and Radio mode.
🔇	Mutes the sound.
←PR	Switches back to previous channel.
INFO	Shows information of the current channel.
MENU	Displays menu on screen, and calls command box.
EXIT	Returns to the previous menu on the menu screen.
ALT-AUDIO	When watching a channel, switches the audio languages.
EPG	Calls up the EPG (Electronic Program Guide)
OK/LIST	Executes the selected item in the menu screen, or enters the desired value in any input mode.
0 - 9	Enter the number in the required menu item or select a channel number to watch.
PR ▲▼	When watching, changes channels, or moves to the next higher or lower item in the menu.
◀ ▶	When watching, adjusts the volume, or moves to the left or right item in menu.
▲▼	Moves up / down a page in the channel list.
PAUSE	Press once to freeze the screen picture. Press once again to go to the normal mode.
L/R	Selects the different audio model.
TXT	Switches to the Teletext mode.
UHF	Switches to the UHF Tuning Mode.
TV/AV	Switches between TV and AV mode.

7. Front Panel

KEY	FUNCTION
⏻/I	Switches between the operational mode and stand-by mode.
▼▲	When watching, changes the channel, or in the menu, moves to the previous and next item.

8. Rear Panel

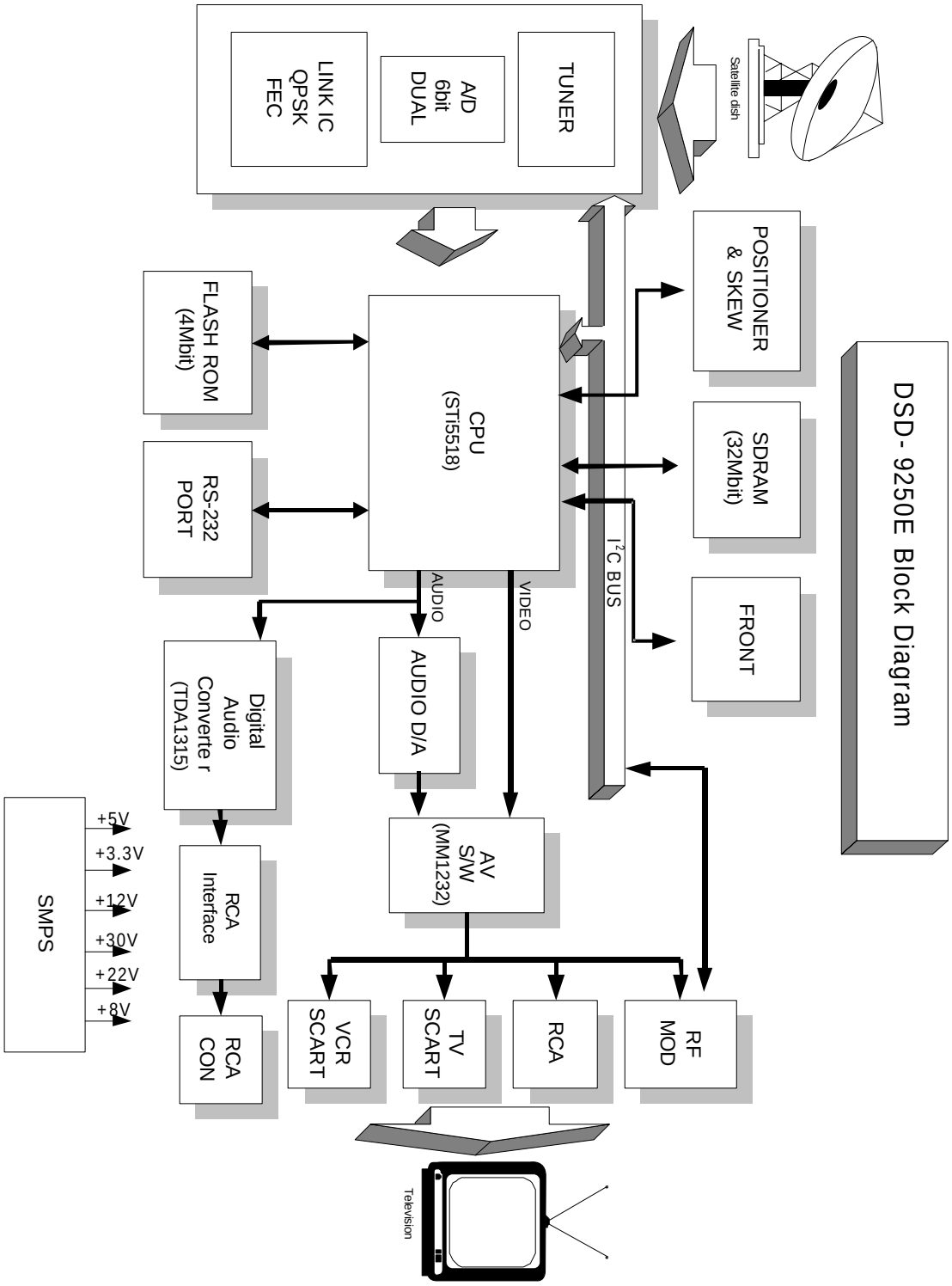


9. Product Specification

System Capabilities	:	Fully DVB compliant
Demodulator		
Waveform	:	QPSK demodulation and FEC decoding in accordance with DVB prETS 300 421
Symbol rate	:	2 < Rs < 45 Msps
Video Decoder		
Decompression	:	MPEG-2 Mian Profile@Main Level
Data rates	:	Up to 60 Mbits/s
Video formats	:	4:3, 16:9
Audio Decoder		
Decompression	:	MPEG laver I and II, Musicam
Outputs	:	Stereo Channel, Dual Mono, Joint Stereo, Mono
Application System Resources		
Microprocessor	:	St Microelectronics STi5518
Clock frequency	:	81 MHz
Flash memory	:	1 Mbyte
SDRAM	:	8 Mbyte
Graphic display	:	720 x 576 (PAL) 720 x 480 (NTSC)
Connector Summary		
LNB	:	1 x LNB input (F-type)
	:	1 x LNB output (F-type : Loop through) : Option
RCA	:	4 x RCA jacks (CVBS, Audio L/R, 0/12V)
SCART	:	2 Scart (TV, VCR)
RS232	:	1 x 9-pin D-sub (Max 625K bits/s)
S-VHS	:	1 x 4-pin Mini Din ; Option
RF modulator	:	PLL or Mechanical type : Option Pll : UHF Channel output (21 - 69 CH) Mechanical : VHF Channel (3 or 4 CH)
LNB & Tuner Input		
Input frequency	:	950 to 2150 MHz
Digital signal input level	:	-65 to -25 dBm
LNB supply	:	13.0 $\pm$ 0.5V / 18.0 $\pm$ 0.7V, max.500mA
Band switch control	:	22 KHz (Microprocessor control)
Connector	:	1 x F-Type, 3/8-32UNEF-2A 2 x F-Type, 3/8-32UNEF-2A (Option)
Power Supply		
Main input voltage	:	90 - 250V AC 50Hz/60Hz
Normal power consumption	:	30W
Remote Control		
Number of keys	:	31 Keys
Operating distance	:	Up to 10m
Front Panel		
Number of keys	:	3 Keys
Indicators	:	power on / Stand by
Display	:	4 Digits (7 segments)
Remote control input	:	Infra-red receiver

Ⅱ. CIRCUIT OPERATING MANUAL

1. Block Diagram



Feature 1. Block Diagram

2. Interface

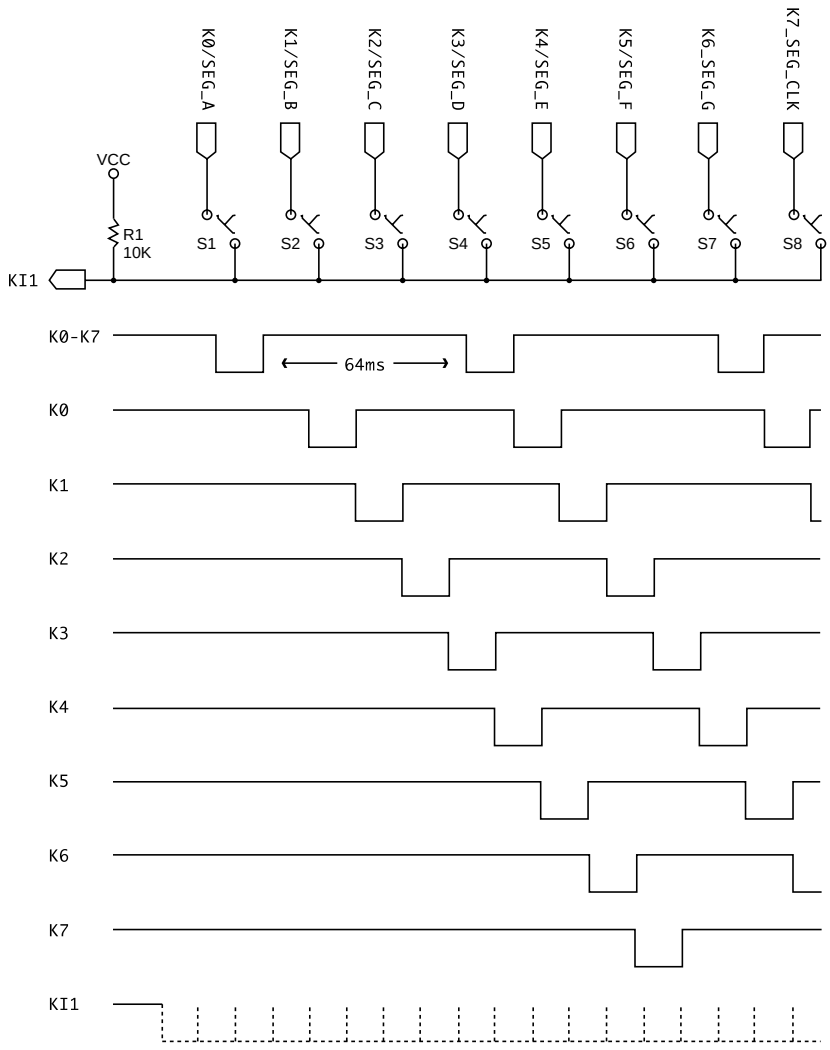
(1) Key Interface

Input can be made by Key using PIO Port for the Key I/O control.

The key value after the scanning is calculated by one Input port and 7 Output Ports.

Output ports are used with the segments of the display.

* Key Scan Method



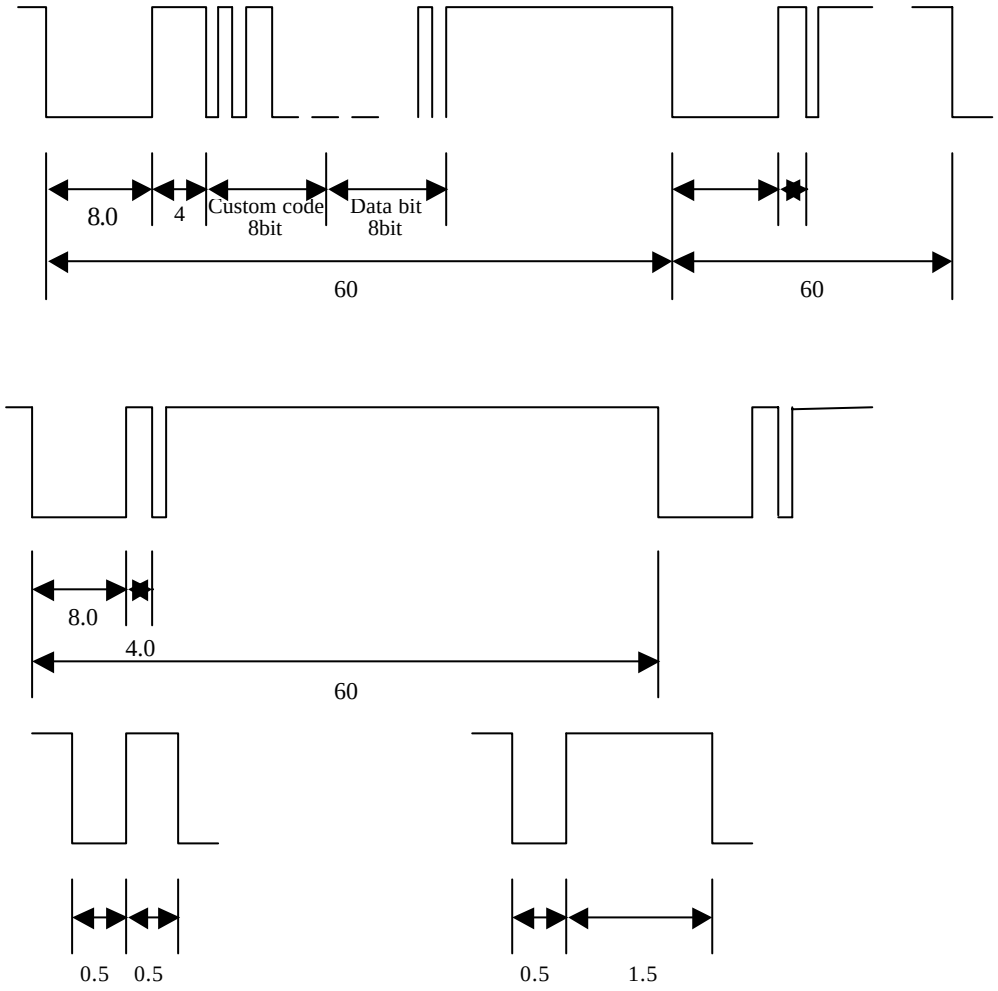
Feature 2. Key Scan

Perform the “Low Scan”,using the Key Output Port(KO0-7) with the cycle of 64ms. If the Key is pressed, the Key Input Port will recognize the status as “low” eventually lead to the key code value while going through the step from K0 to K7.

(2) Remote controller Interface

Recognize the REMOCON Code value after analyzing Interrupt Interval Time through PIO Port that reads the output signal of the IR sensor.

MITSUBISH formats were used for the REMOCON signal. Following is the Timing Diagram for the MITSUBISH signal format.



Feature 3. MITSUBISH Format Timing

The signals are made up of Leader Code, Custom Code (8bit), Separator and Data Code (8bit). Following is the value of the individual Key.

Chart 1. Remote controller Key Code

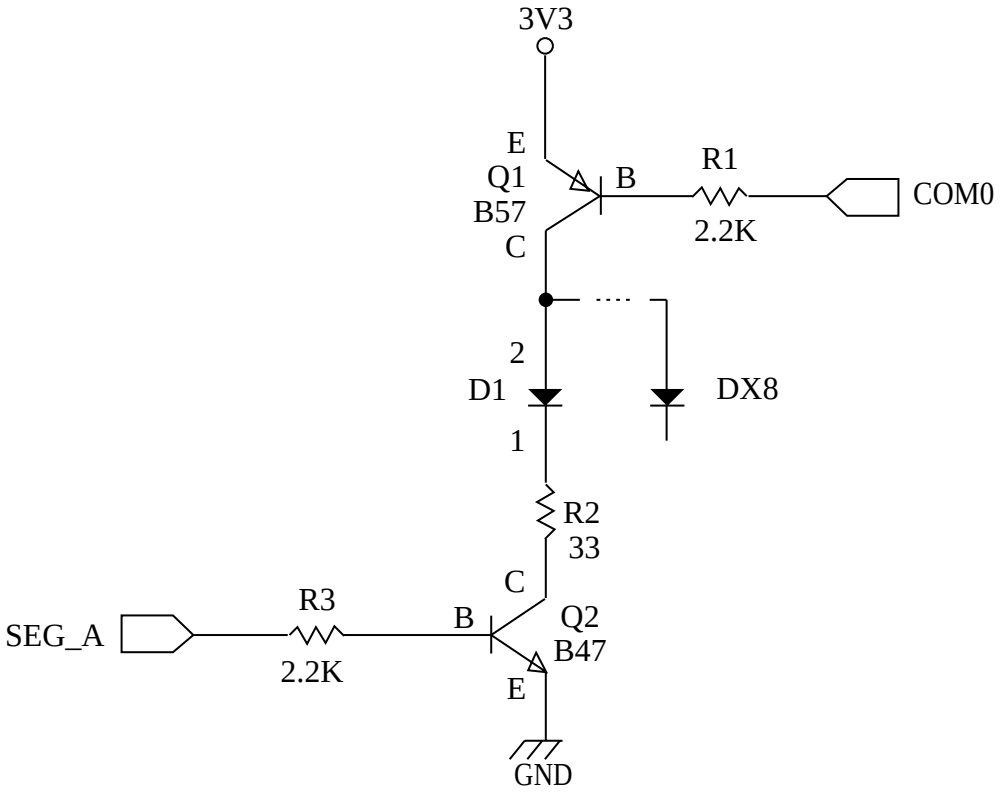
Key Function	Hex	Key Function	Hex
Custom code	0x16	∩	0x1C
Power	0x15	INF0	0x21
Mute	0x12	PRπ	0x17
1	0x01	PRθ	0x18
2	0x02	τ	0x14
3	0x03	υ	0x13
4	0x04	OK	0x11
5	0x05	EXIT	0x23
6	0x06	∪	0x1D
7	0x07	EPG	0x24
8	0x08	PAUSE	0x1E
9	0x09	Audio-L/R	0x0D
0	0x00	ALT-AUDIO	0x0E
TV/RADIO	0x0A	TXT	0x25
∧PR	0x20	UHF	0x26
MENU	0x22		

(3) Display Interface

The signal that controls the Segment of 7-Segment is used with the signal of Key Scan as mentioned above in Key Interface section.

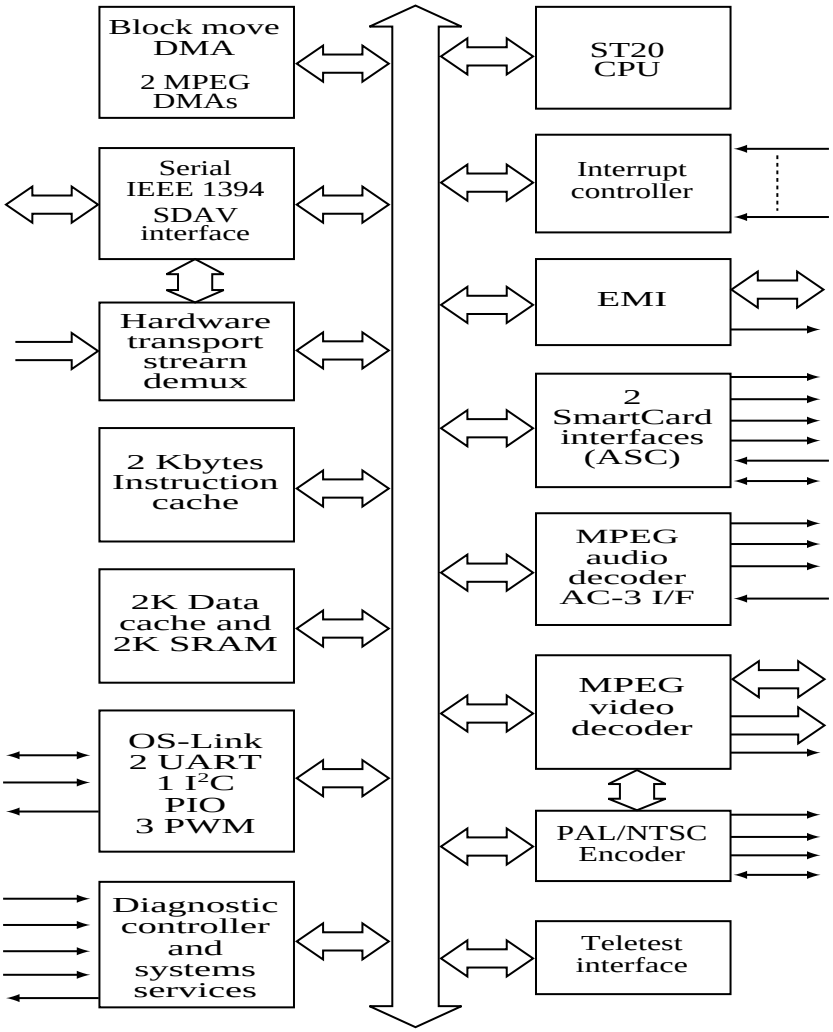
Common signals that control Digit use PIO (PIO3-0,1,2,3 and 4)

Following picture shows the structure of operation. Display use Common Cathode Type. Display is activated by recurrent signals with cycle of 1~3ms.



3. Peripheral device of STI5518

(1) Structure



Feature 5. Sti5518 Block Diagram

STI5518 is a 1 chip including 32bit RISC CPU, A/V Demux, Video Encoder, Multi PIO and Cache RAM for the use of DVB and DSS Set Top.
Followings are summary of distinctive features of each Block.

- ■ Enhanced capability with 32bit VL-RISC CPU Core of 81MHZ clock.
- ■ Supporting Bandwidth of 200MB/S using internal 2KB SRAM buffer and 2KB DCACHE.
- ■ Video Decoder is attached inside supported by MPEG-2 MP@ML and Letter Box.
- ■ MPEG Layer1 and 2 Audio Decoder are stored inside.
- ■ Providing interface external AC3 Decoder.
- ■ Supporting 2 - 8bit/pixel OSD.
- ■ Internally stored Video Encoder for the output of RGB, CVBS and Y/C Video
- ■ Enhanced CPU and Decoder capability boosted by 64Mbit SDRAM.
- ■ Backing External Surrounding Interface Memories. (4 Banks)
- ■ Able to use Hardware DMUX, input Serial and to support 32Pid.
- ■ Boosting 8 Level INT.
- ■ Supporting DMA and other multi PID.

(2) Reset Section.

If the Low signal is read by Sti5518의 Reset Pin, the Register value of all Sti5518 will be initialized.
There must be at least of 8 clock (37nsec) of Reset Time.

Feature 6. Reset Timing

(3) Clock Section.

STI5518 has two PLL inside. Operative clocks are made by external clock with one unit of 27MHz. The two PLL are as of ST20 PLL and MPEG PLL.
ST20 PLL produces 81MHz of system clock that is to be used in processor and peripheral equipment.
MPEG PLL produces audio decoder system clock, audio PCM clock, TS Demultiplexer and memory clock of SDRAM.
27MHz clock uses VCXO. Currency control is enabled by PWM OF Sti5518의 PWM with the reference of the PCR value of MPEG to set the exact initiative of MPEG. If this value is not appropriate the colors are not be seen on the screen, or the screen will display broken features.

(4) PIO Structure.

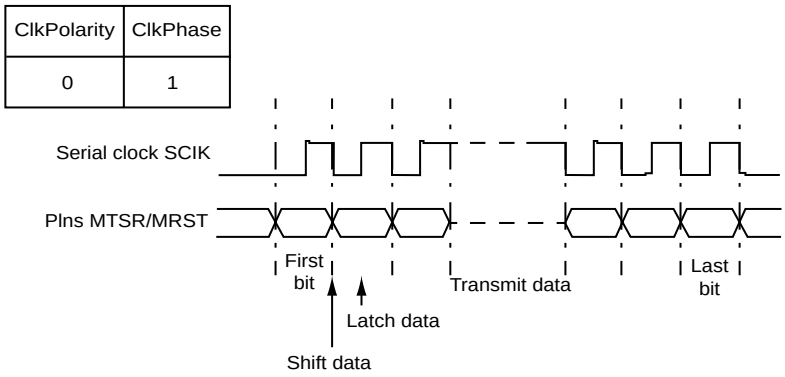
Sti5518 supports PIO that back up 5 number of Ports (8bit) as of PIO0, PIO1, PIO2, PIO3 and PIO4. Some ports are able to endow extra functions to PIO for flexible expansion in usage. Following chart shows Alternative Function Pin of PIO.

Port bit	Alternative function of PIO pins				
	PIO port 0	PIO port 1	PIO port 2	PIO port 3	PIO port 4
0	ASC0TxD or Sc1DataOut	SSC0 MTSR	ASC2TxD or Sc0DataOut		
1	ASC0RxD or Sc1DataIn	SSC0 MRST	ASC2RxD or Sc0DataIn		
2	Not connected	SSC0 SCIK	Not connected		
3	Sc1Clk	CaptureIn1	Sc0Clk		
4	(Sc1RST)	CaptureIn2	CompareOut0 (Sc0RST)		
5	(Sc1CmdVcc)	ASC1TxD	(Sc0CmdVcc)		CompareOut1 (IROut)
6	ASC0Dir	ASC1RxD	Not connected	TriggerIn	CaptureIn3
7	(Sc1Detect)	ASC3TxD	CaptureIn0 (Sc0Detect)	TriggerOut	ASC3RxD

Chart 2. PIO Alternate Functions.

This section only provides summaries of individual function of each Port.
Further discussion will be followed in individual port section.

- I^2C_DATA (PIO1_0)
- I^2C_CLK (PIO1_2)
  Used for the transmission of Serial and control of Tuner, CI-Max, AV Switch and RF Modulator.



Feature 7. I^2C Timing

PIO	NAME	I/O	Function	Remarks
PIO1_0	I2C_Data(SSC0)	I/O		
PIO1_2	I2C_Clk	O		
PIO1_3	NOTPGM_EN	O	L:Flash program enable	
PIO1_4	SLOW_S/W	I	H:VCR Scart Input ON L: VCR Scart Input OFF	
PIO1_5	RS232_Tx	O		
PIO1_6	RS232_Rx	I		
PIO2_7	KI1	I		
PIO3_0	COM0	O		
PIO3_1	COM1	O		
PIO3_2	COM2	O		
PIO3_3	COM3	O		
PIO3_4	COM4	O		
PIO3_5	Seg_clk/K7	O		
PIO3_6	TriggerIN	I		
PIO3_7	TriggerOUT	O		
PIO4_0	SegA/K0	O		
PIO4_1	SegB/K1	O		
PIO4_2	SegC/K2	O		
PIO4_3	SegD/K3	O		
PIO4_4	SegE/K4	O		
PIO4_5	SegF/K5	O		
PIO4_6	REMOCON_IN	I		
PIO4_7	SegG/K6	O		

Chart 3. PIO Map

- NOTPGM_EN (PIO1_3)
  Flash ROM Write protect/ Program enable (Low) or Program disable (High)
- SLOW_S/W (PIO1_4)
  Checking the connection of external features with Vcr scart such as VCR and general power on/off status. Connect and power on(High), Not connect or power off(Low)
- RS232_Tx (PIO1_5)
- RS232_Rx (PIO1_6)
  Rs232 serial data transfer (Used to S/W upgrade, Debugging)
- KI1 (PIO2_7)
  Key input check. Reading Keys when in the Low status.
- COM0 (PIO3_0)
- COM1 (PIO3_1)
- COM2 (PIO3_2)
- COM3 (PIO3_3)
- COM4 (PIO3_4)
  Selecting 4 Digit of the Display, including clock dots. If it's in Los status, the Digit will be in ON status.
  SegA/K0 (PIO4_0)
- SegB/K1 (PIO4_1)
- SegC/K2 (PIO4_2)
- SegD/K3 (PIO4_3)
- SegE/K4 (PIO4_4)
- SegF/K5 (PIO4_5)
- SegG/K6 (PIO4_7)
- Seg_clk/K7 (PIO3_5)
  Signals the segment of Display and Dot (is ON when in High status) and Key Scan.
- Trigger IN (PIO3_6)
- Trigger OUT (PIO3_7)
  Used when debugging with DCU Tool
  REMOCON_IN (PIO4_6)
  Recognize the REMOCON signal being sent from IR Sensor.

(5) Memory Interface

Sti5518 can support both On-chip memories that are 2KB SRAM, 2KB SRAM or Data Cache and 2KB Instruction Cache and external expanded memories as of ROM and DRAM. Moreover, SDRAM can be used up to 32Mbits with MPEG memory. From the 32Mbits SDRAM 16Mbits can be used as the buffer of MPEG and the rest of 16Mbits can be used as Code buffer enabled by Code on SDRAM program.

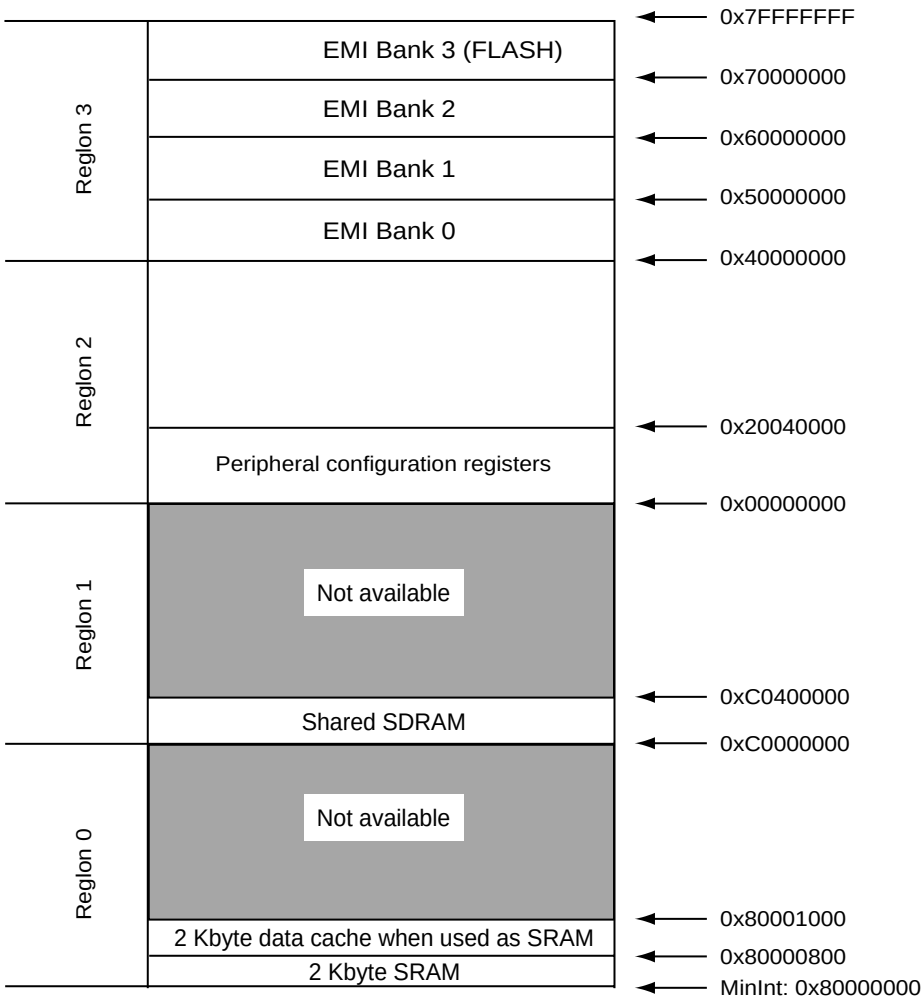
A. REGION 0
   On-Chip memory, Handler, Trap and DMA are allotted from the address 0X80000000 to 0XBFFFFFFF.

B. REGION 1
   From the address 0XC0000000 to 0XC0400000 are used as a buffer memory of MPEG.

C. REGION 2
   From the address 0X00000000 to 0X3FFFFFFF, they're used for the surrounding area for the internal parts. Individual part has 4Kbyte.

D. REGION 3
   EMI (Extended Memory) is divided to 4 Banks. Bank 0 is only applicable for the DRAM Interface.

Following is the Memory MAP Table.



Feature 8. Memory Map

The size of EMI Bus is 16bit and also support for the 8bit Bus. The Bank0 of EMI can support DRAM Interface while rest of Bank as of Bank1, 2 and 3 can only support SRAM, ROM and Peripheral Interface.

- Data 0 - 15
  16bit data transfer
- Adr 1 - 21
  When using DRAM, it supports Multiplex mode (Row and Column Address) with the access ability of 32bit.
- not_WE0
- not_WE1
  Signals individual bite Enable Strobe when addressing 2bit word at EMI.

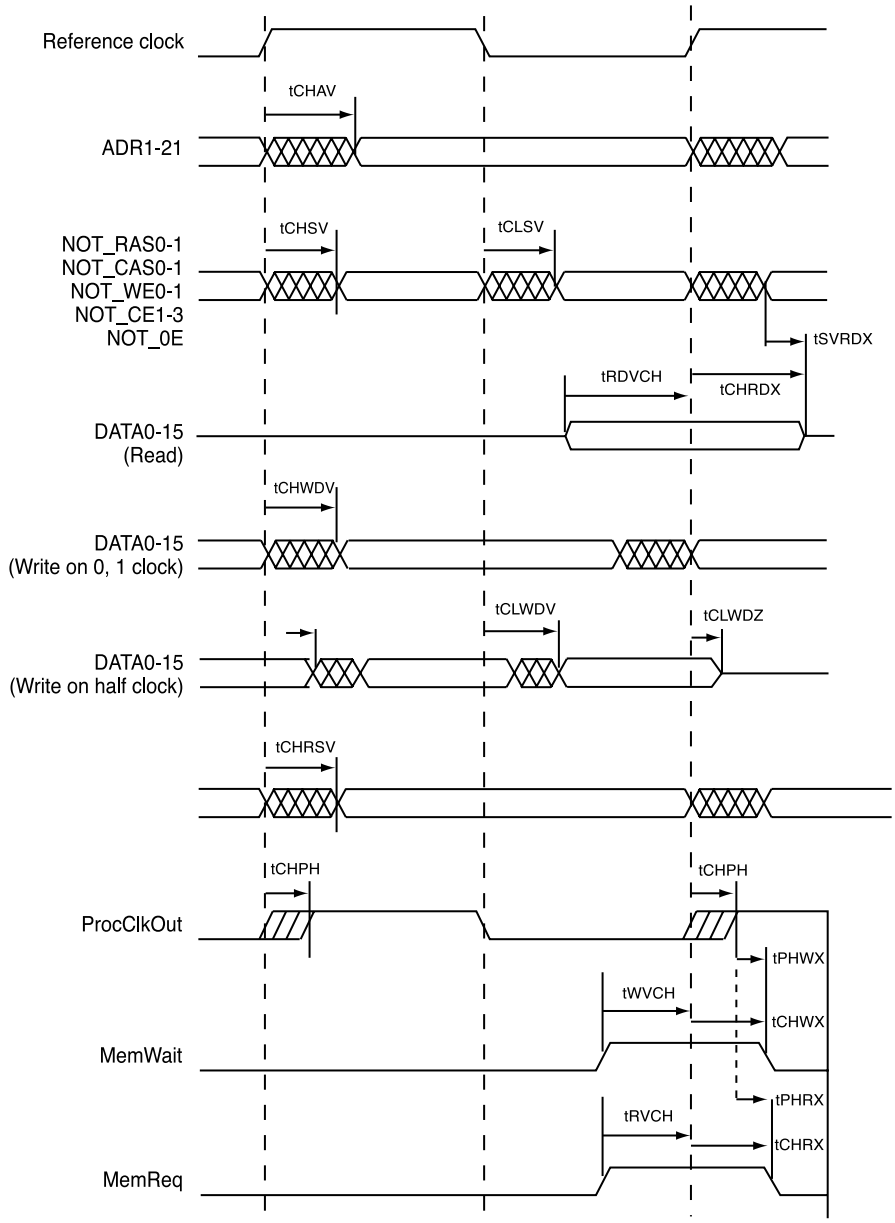
  Not_WE0 assert : Data 0 - 7 enable
  Not_WE1 assert : Data 8 - 15 enable
- not_CE0
- not_CE1
- not_CE2
- not_CE3
  EMI Bank0/1/2/3 Chip select strobe

- MemWait
  Wait signal is produced in external device when accessing SRAM and peripheral devices. Wait signal is maintained as Order status in the High status motivated by processor clock.
- Not_OE
  Read Strobe
- ReadnotWrite
  The ability to Read or Write of processing cycle.

Symbol	Parameter	Min	Max	Units	Note
tCHAV	Referecne Clock high to Address valid	-8.0	0.0	ns	
tCLSV	Reference Clock low to Strobe valid	-8.0	3.0	ns	
tCHSV	Reference Clock high to Strobe Valid	-8.0	0.0	ns	
tRCA/CH	Read Data valid to Reference Clock high	13.0		ns	
tCHRDX	Read Data hold after Reference Clock high		-2.0	ns	
tSVRDX	Read Data hold after Strobe valid	0.0		ns	1
tCLWOV	Reference Clock low to Write Data valid	-8.0	7.0	ns	1
tCHWOV	Reference Clock high to Write Data valid	-8.0	6.0	ns	1
tCHWDZ	Reference Clock high to Write data tristate	-8.0	6.0	ns	
tCHRSV	Reference Clock high to remaining Strobes valid	-8.0	3.0	ns	
tCHPH	Reference Clock high to **ProcClkOut** high	-8.0	0.0	ns	
tWVCH	**MemWait** valid to Reference Clock high	13.0		ns	
tRVCH	**MemReq** valid to Reference Clock high	13.0		ns	
tRHWX	**MemWait** hold after **ProcClkOut** high	0.0		ns	1
tPHRX	**Memreq** hold after ProcClkOut high	0.0		ns	1
tPHEMIZ	**MemGrant** to signals tristate when bus granted	TBD		ns	1

Chart 4. EMI Timing Value

Access cycle of EMI Bank3 and Bank2 is as following feature. The value of timing chart can be modified by the value of Configuration Register setting.

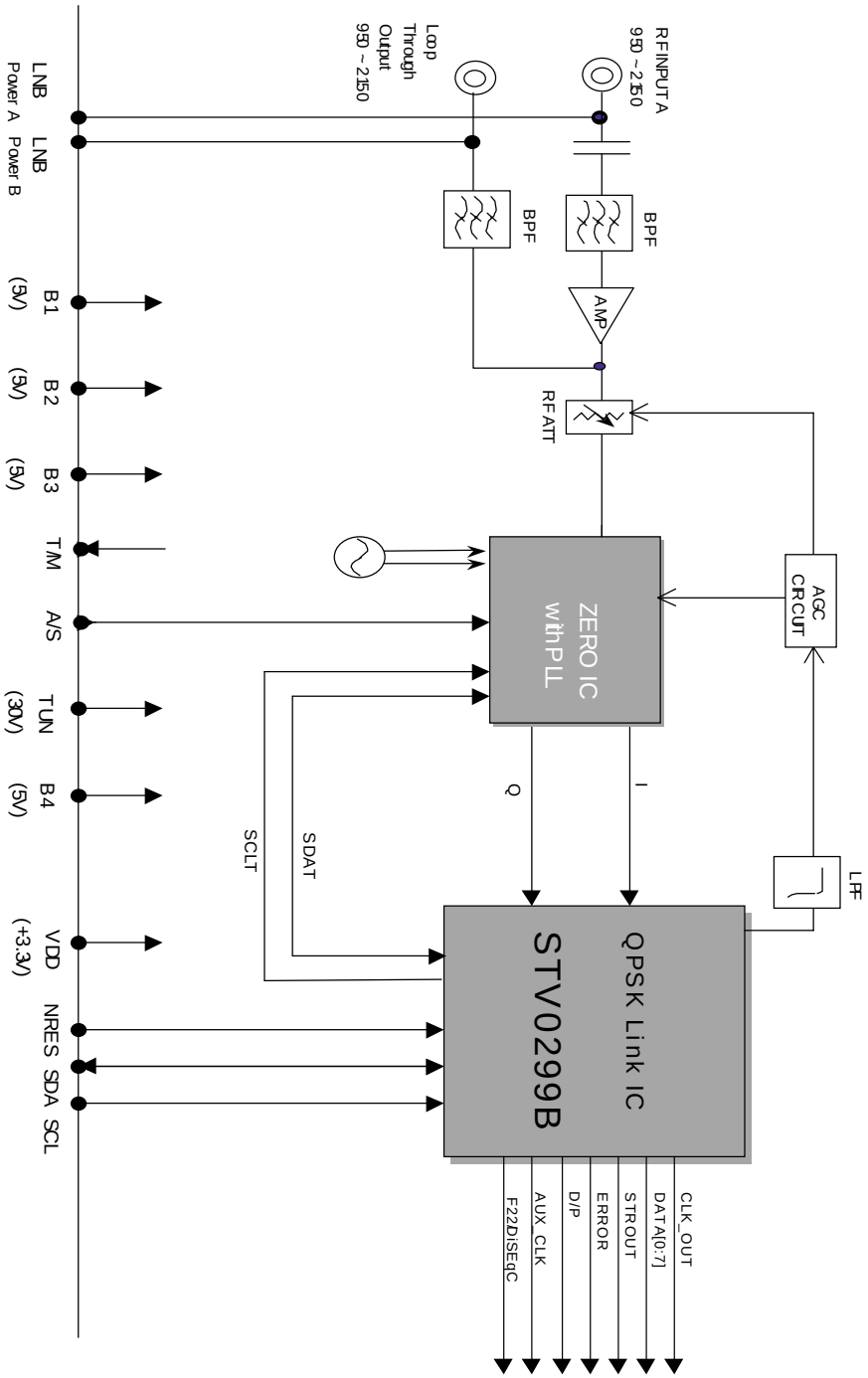


Feature 9. EMI Interface Timing

4. Front-End Interface

(1) Tuner Module

Tuner and QPSK Demodulator are combined into one Module. Following feature shows the Block Diagram.



Feature 10. Tuner Modul Block

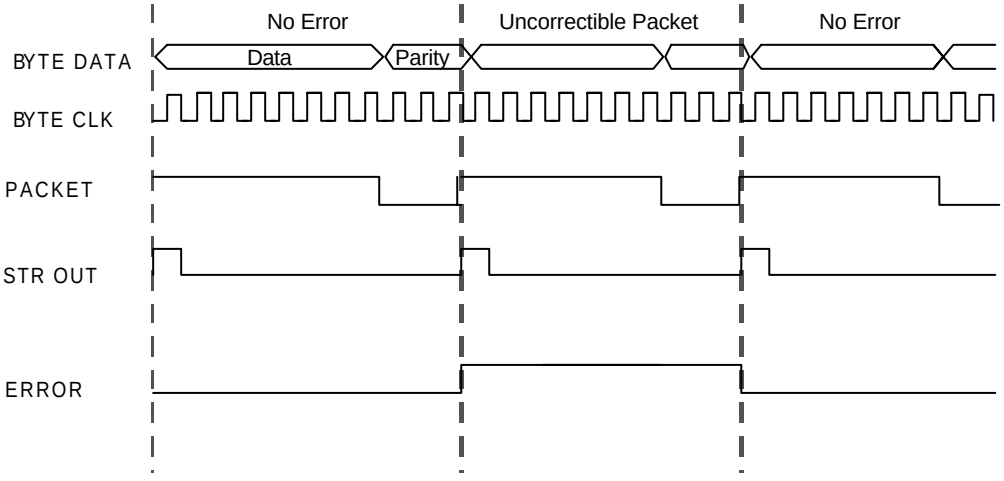
* The functions of individual Pin.

PIN NAME	PIN No.	PIN DESCRIPTION
LNB POWER B	1	LNB Voltage supply. To put 1000PF of ceramic capacitor into ground.
LNB POWER A	2	LNB Voltage supply. To put 1000PF of ceramic capacitor into ground.
A-GND	3,6	GND. Please don't let any Digital Noise enter through ground.
B1	4	5V Supply for RF Amp TR
B2	5	5V Supply for ZERO-IF chip(for RF)
B3	6	5V Supply for ZERO-IF chip(for PLL)
A/S	8	I^2C Bus Address selection input (See table 3)
T/M	9	Tuning voltage monitor (Do not connect it to anywhere)
TUNING(+30V)	10	PLL channel select voltage supply (+30V)
B4	11	5V supply for AGC pull-up
NRES	12	Reset, active at low level.
AUX_CLK	13	Programmable Output Port or Programmable Output Clock
F22/DiSEqC	14	DiSEqC modulation (22kHz Tone), Programmable Output Port
SCL	15	I^2C Bus
SDA	17	
N.C	16	Do not connect it to anywhere
BCLK OUT	18	Output Byte Clock; or Bit Clock in Serial Mode.
N.C	19	Do not connect it to anywhere
DO,....,D7	20~27	Output Data : D7 is DATA_OUT in Serial Mode.
N.C	28	Do not connect it to anywhere
D/P	29	Data/Parity Signal.
ERROR	30	Output Error Signal. Set in case of uncorrectable packet.
STR OUT	31	Output 1st byte Signal (synchro byte clock)
VDD	32	+3.3V Supply for LINK IC

Chart 5. Tuner Module Pin Out

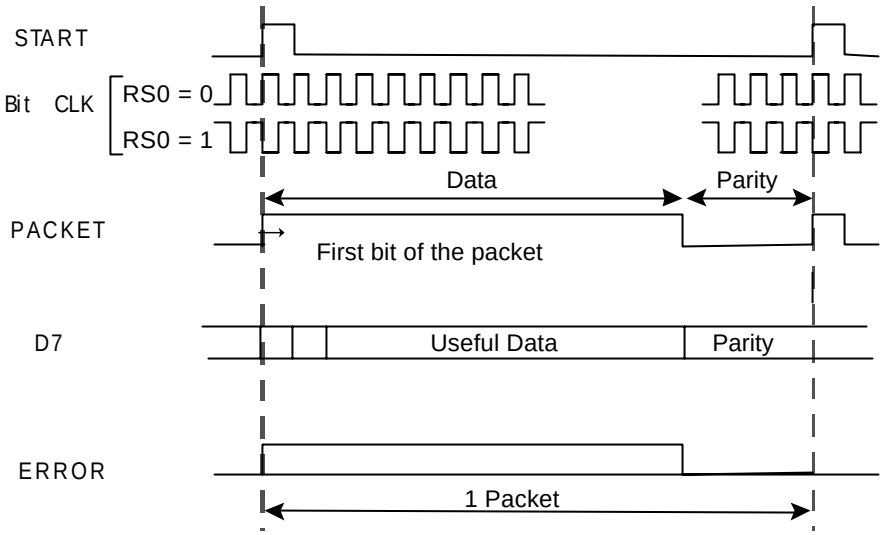
TS Output is made by the Serial or Parallel function.
The relationship between TS output Data and Control signal is showing in the following diagram. If an error occurs Data is ignored, and the Data in the Valid area is valid.

● Parallel Output Timing



Feature 11. Parallel Data Output Timing

● Serial Output Timing



Feature 12. Serial Data Output Timing

(2) Related with LNB.

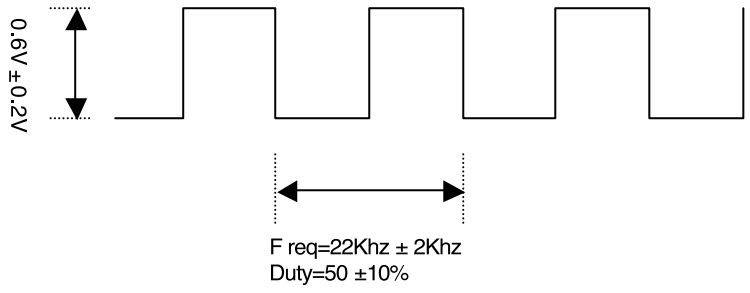
1) LNB power and 22khz Tone Pulse
The power supplied to LNB sends the 22Khz Tone signal that is used in horizontal(18V), vertical(13V) and frequency Band and Diseqc Command.

UNI-CI Model uses LNBPIO series that are exclusive IC for the LNB from ST company.
Control signal is sent through 74HC574(IC5and IC6) from CPU.

Chart 6. LNB Control signals

Function	High	Low
H/V	Horizental(18v)	Vertical (13v)
22Khz-ON	22Khz ON	22Khz OFF
LNB-ON	LNB ON	STD BY
AUX/IRD (Loop Through)	IRD MODE	AUX MODE (External SAT)

22KHZ Tone Spec is



Feature 13. 22Khz Tone Pulse

2) Loop Through

Supports Loop Through for the Interface function of other Satellite Devices. That means, in other Satellite device, the control of LNB related voltage and Tone are possible.

If the signal of AUX/IRD Control is in “High” status, the LNB voltage is provided from LNBP. If it’s in Low, the power can be supported from the external device in the Default states.

5. A/V Interface

(1) Video

Sti5518 has internal Digital Encoder of PAL/NTSC.

Digital Encoder can modify the Digital Video Stream with the ration of 4:2:2 or 4:4:4, OSD, Sub-picture and produce Analogue Base band PAL/NTSC signal and RGB signal.

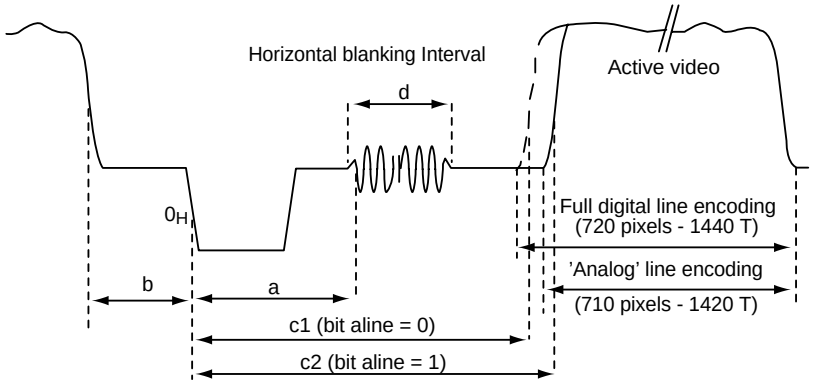
Encoder output supports Interlace mode or Non-interlace mode.

There are 6 Pins for the Analogue Video output. (CVBS, S-VHS(Y/C), RGB)

Moreover, it supports Teletext, closed-captions and CGMS.

Following picture shows the signal formats from the individual output.

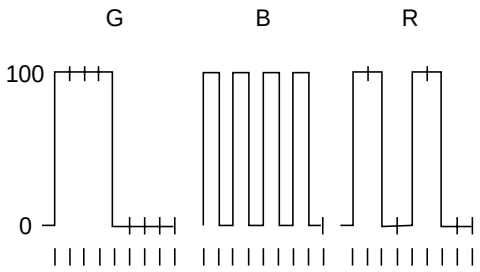
1) CVBS Timing



	NTSC-M	PAL-BDGHI	PAL-N	PAL-M
a	5.38 µs (even lines) 5.52 µs (odd lines)	5.54 µs (A-type) 5.66 µs (B-type)	5.54 µs (A-type) 5.66 µs (B-type)	5.73 µs (A-type) 5.87 µs (B-type)
b	1.56 µs	1.28 µs	1.28 µs	1.28 µs
c1	8.8 µs	9.3 µs	9.3 µs	9.3 µs
c2	9.3 µs	10.1 µs	10.1 µs	10.1 µs
d	9 cycles of 3.58MHz	10 cycles of 4.43MHz	9 cycles of 3.58MHz	9 cycles of 3.58MHz

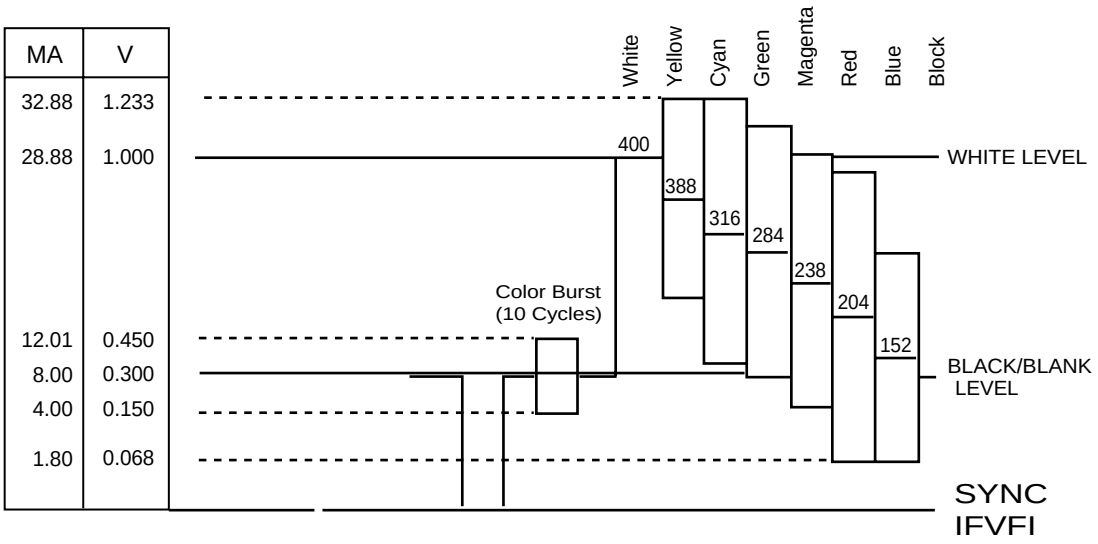
Feature 7. CVBS Timing

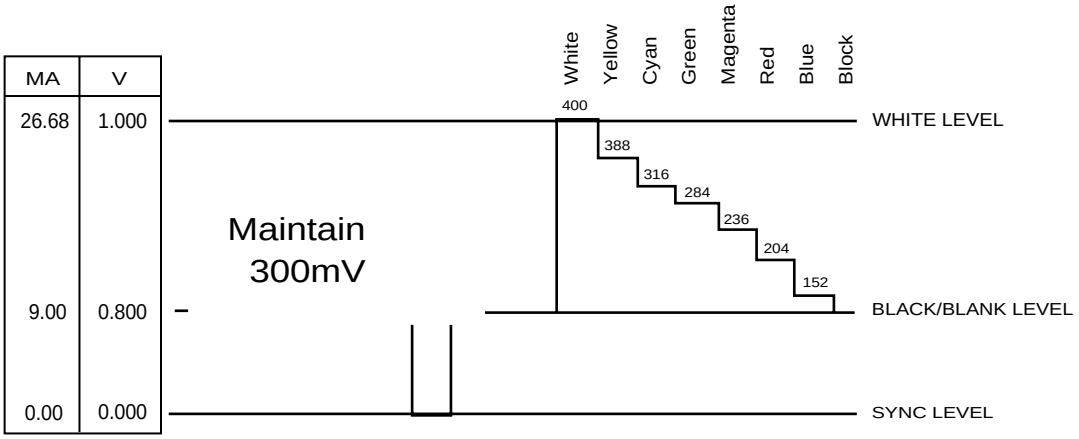
2) Comparison of RGB signals.

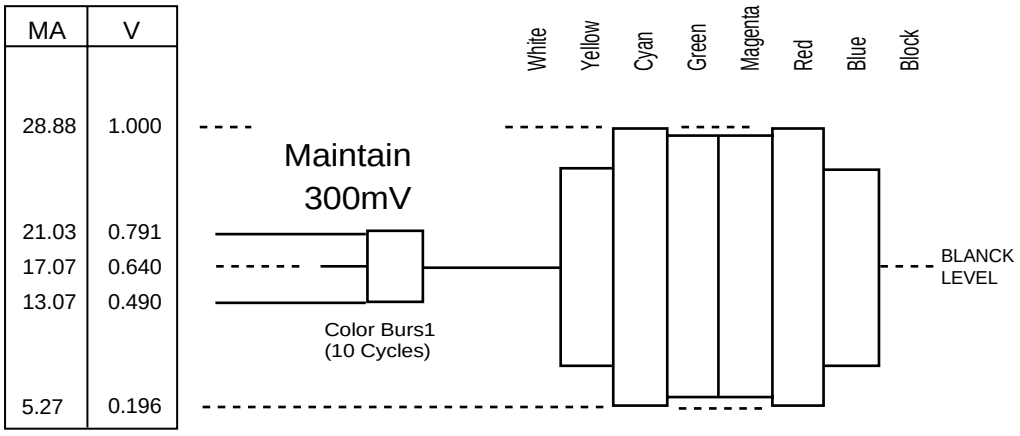


Feature 8. RGB Signal Pulse

3) Color Bar CVBS, Y, C, signals







Feature 9. CVBS, Y and C Waveform of Color Bar signals

1-4) Video Output

There are 5 Video Output Port in the DSD-9250E products. (TV Scart, VCR Scart,S-VHS,RCA JACK, RF_MODULATOR)

The output of R,G and B signals are sent to TV Scart through Video Buffer and LPF (Low Pass Filter) originated from the STI5518 output.

Y and C signals output is sent to S-VHS JACK through Video Buffer and LPF from the Sti5518 output.

CVBS signal output takes place in VCR SCART through the Video Buffer and LPF from the STI5518 output. Moreover, the CVBS signals from the STI5518 output is sent to the INPUT of A/V SWITCH(MM1232) for the Switching (SAT MODE/VCR MODE SELECT) with CVBS signals that were entered from the VCR SCART. A/V SWITCH (MM1232) selects Output depends on the Logic status of Pin (2,7 and 12). Selected signals in the A/V SWITCH system is sent to individual output mode of TV SCART, RF_MODULATOR and RCA JACK through the Video Buffer and LPF.

There are two control signals as of Fast Blanking and Slow Blanking in TV SCART.

Chart 9 shows the usage of control signals.

Slow Blanking (Pin8)	- Can select either TV/AV mode or 16:9/4:3 mode.	
	TV/AV	Selecting TV/AV mode of TV SET. TV mode : <1.5V, AV mode : 10 ~ 12V
	16:9/4:3	Selectint Wide Mode. 4:3 mode = 10 ~ 12V, 16:9 mode= 5 ~ 6.5V
Fast Blanking	Select video input signal of TV. RGB : 1~ 3V CVBS : 0 ~ 0.4V	

Chart 9. Slow/Fast Blanking Function

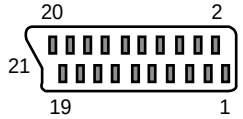
Current TV/VCR Scart Pin that are used in the DSD-9250E is as following.

FUNCTION	PIN NO.
AUDIO_OUT_R	1
AUDIO_OUT_L	3
VIDEO_OUT	19
SLOW_SWITCH	8
FAST_BLANKING	16
R	15
G	11
B	7
VIDEO_GND	5,9,13,14,17,18,21
AUDIO_GND	4

FUNCTION	PIN NO.
AUDIO_OUT_R	1
AUDIO_IN_R	2
AUDIO_OUT_L	3
AUDIO_IN_L	6
SLOW_SWITCH	8
VIDEO_OUT	19
VIDEO_IN	20
VIDEO_GND	5,9,13,14,16,17,18,21
AUDIO_GND	4

Chart 70. TV/VCR SCART Connector Pin

Following Table shows the Scart Connector



(SCART CONNENTOR)

Pin	Name	Description	Signal Level	Impedance
1	AOR	Audio Out Right	0.5 V rms	<1k ohm
2	AIR	Audio In Right	0.5 V rms	>10k ohm
3	AOL	Audio Out Left + Mono	0.5 V rms	<1k ohm
4	AGND	Audio Ground		
5	B GND	RGB Blue Ground		
6	AIL	Audio In Left + Mono	0.5 V rms	>10k ohm
7	B	RGB Blue In	0.7 V	75 ohm
8	SWTCH	TV/AV(4:3, 16:9) Mode Select		
9	G GND	RGB Green Ground		
10	CLKOUT	Data 2: Clock pulse Out (Unavailable ??)		
11	G	RGB Green In	0.7 V	75 ohm
12	DATA	Data 1: Data Out (Unavailable ??)		
13	R GND	RGB Red Ground		
14	DATAGND	Data Ground		
15	R	RGB Red In / Chrominance	0.7 V (Chrom.: 0.3 V burst)	75 ohm
16	BLNK	Blanking Signal	1-3 V=RGB, 0-0.4 V=Composite	75 ohm
17	VGND	Composite Video Ground		
18	BLNKGND	Blanking Signal Ground		
19	VOUT	Composite Video Out	1 V	75 ohm
20	VIN	Composite Video In / Luminance	1 V	75 ohm
21	SHIELD	Ground/Shield (Chassis)		

Chart 81. SCART PINSPEC.

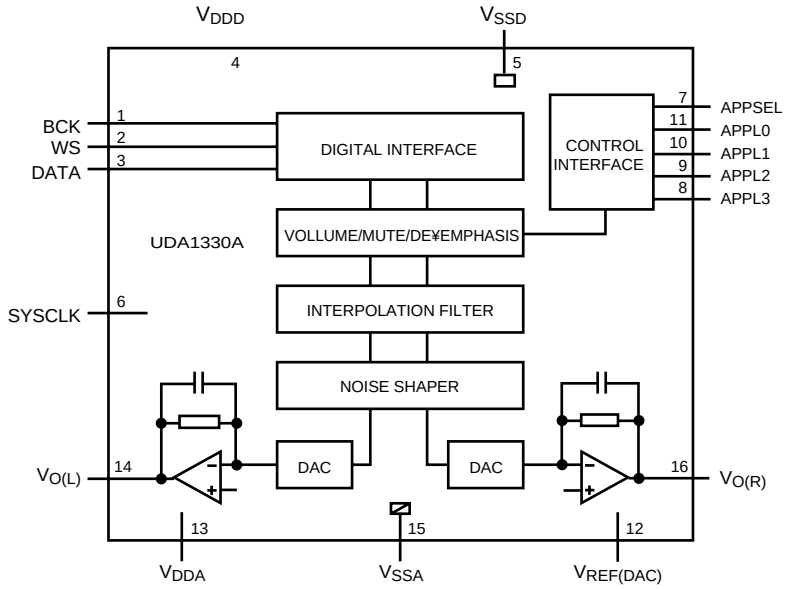
(2) Audio

1) PCM Audio

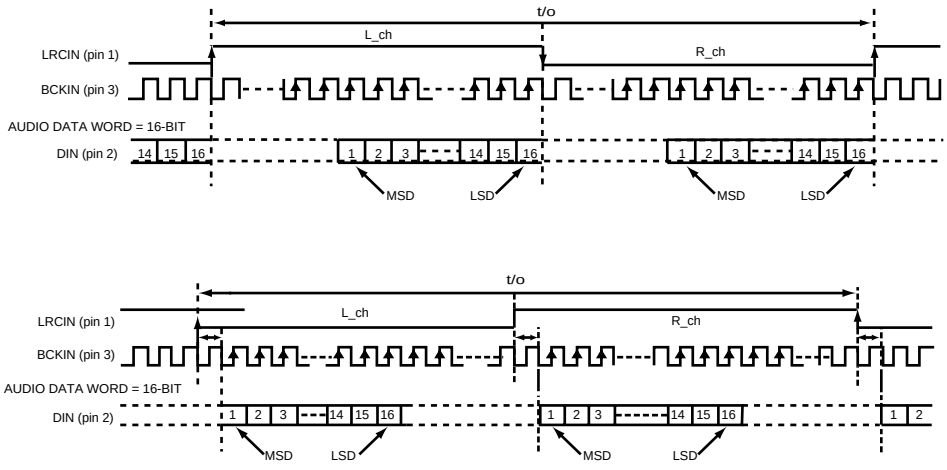
Audio related output of the Sti5518 is made in the form of PCM format and AC3 Interface format.
DSD-9250E uses the serial data of PCM format. PCM Data output format is in Standard format and I2S Compatible PCM format.
Followings are the interface signals of PCM format.
PCMDATA (Sti5518 Pin44) : PCM Serial Data Output

- SCLK (Sti5518 Pin43) : PCM Clock Output
- LRCLK (Sti5518 Pin46) : Left/Right Channel select
- PCMCLK (Sti5518 Pin45) : PCM Clock Input(18.432Mhz)

Data of PCM format is modified to Analogue signals at the external Audio DAC. The output information is sent to external output port through Output magnifying equipment and AV Switch.
DSD-9250E can use two Audio DAC systems. (CS4331/Crystal, UDA1330/Philips)
Following diagram shows Timing Diagram with Audio DAC and Philips UDA1330 Block.



Feature 10. Audio DAC(UDA1330) Block



Feature 11. PCM Timing

Analogue Audio Signals that are modified at Audio DAC are amplified by three times after going through Low Pass Filter. The output is made after the amplification through AV Switch or Buffer.
In DSD-9250E, use the AV Switch (MM1232). Refer the A/V switch in the previous section of Video Explanation.

2) Digital Audio(SPDIF Format)
Use TDA1315/Philips which are IC of the Digital Audio Encoding system in 'SPDIF' format. The signals are entered from the PCM Format (I2S Format).
The Digital Signals that were encoded in SPDIF go through driver circuit, then the output is placed in the RCA unit. This output will be connected with Digital Audio Devices.

6. Software Operating Steps

(1) Operating Steps.

A. Initialize multi-purpose PIO port
B. STI5518 chip version detection
C. Set DMT default multi-purpose PIO port
D. Initialize the OS20 software scheduler
E. Initialize the interrupt subsystem
F. Flash vendor check
G. Booting mode check(UART Debugging mode / Factory Test Mode / Normal Mode)
H. develop_init
I. i2c_init
J. pti_init
K. pwm_init
L. pcr_init
M. tuner_init
N. uart_init
O. mpeg_init
P. gprim_init
Q. teletextInit
R. run_smallwin
S. front_init
T. AudioPesManagerInit

(2) Normal States after the Power On

1) 'BOOT' is displayed on the Front Panel.
➔ Boot Loader is activated having following functions.
System Booting
Flash Memory & Program Check
System Upgrade by another DSR or PC
Factory Default Data read/write by PC

2) '----' sign is displayed in Front Panel.
➔ Check whether the User Data is being loaded to Main RAM from the Flash ROM. Check the validity of Data.

(3) UART Console Message

Following Booting Message will be seen after executing UART Emulator Program when connecting RS232C Port with PC.

1) Development environment display

```
************************************************************
    STi5518 DVB Reference Firmware Version 6.0
    Code Exe = 0x4d4f52  (ROM)
************************************************************

Software compiled on Apr 04 2000 at 01:33:58
With DCU release 1.6.2 (50600)
ANSI C compiler  Version  5.06.00 (04:41:24 Oct 15 1998)  (W95/NT-PC)
OS20 kernel 2.05.03 (12:07:34 Oct 19 1998)

Device_id = 2d4c9041 (STi5518)  (STi5518 version E, F or G detected)
[VID_REV=D1]        [AUD_REV=D3]
[DENC_CHIPID=53]    [DENC_REVID=00]

--- General configuration ---
  Instruction cache Enabled
  [TESTTOOL_PRESENT fitted]
  [EVAL5518        NOT fitted]
  [CODE_ON_SDRAM    fitted]
```

--- DEVELOP driver configuration ---
[UARTIO fitted]
[UNHOSTED NOT fitted]
[STREPORT fitted]

--- MPEG driver configuration ---
[B_ON_THE_FLY fitted]
[ENABLE_AVSYNC fitted]
[DONT_BLOW_UP_HALF_SIZE_PICTURES NOT fitted]
[BUILT_FOR_16MBIT fitted]
[DECODE_ELEMENTARY_STREAM NOT fitted]
[SIF_UPSAMPLING_WORKAROUND NOT fitted]

2) I2C driver initialized message

I2C driver initialized

3) API Information & Clock Initial

CFG_DRC = 0x2b
PTI driver library v3.0
Link I/F cut 2.x initialized for DVB
Setting up the link i/f interrupt
Clock recovery/PWM init
[PWM_REBASING FITTED]
[PWM_CONTROL_LARGER_VALUE_FASTER_CLOCK FITTED]
[PWM_INITIAL_VALUE: 0x83]
PCR init

4) Tuner Initial

TUNER Module Initialization
Creating TUNER module semaphores ...

module_type = 148 Successfully Installed TUNER module

5) MPEG SDRAM configuration

MPEG SDRAM configuration :
Video Bit Buffer : Size= 400 Kbytes From 0xc0000000 to 0xc0063fff
Audio Bit Buffer : Size= 16 Kbytes From 0xc0064000 to 0xc0067fff
OSD Buffer : Size= 400 Kbytes From 0xc0068000 to 0xc00cbfff
Frame Buffer A : Size= 608 Kbytes From 0xc00cc000 to 0xc0163fff
Frame Buffer B : Size= 608 Kbytes From 0xc0164000 to 0xc01fbfff

First free address = 0xc01fc000
Total SDRAM used = 2032 Kbytes
SDRAM not used by MPEG = 16 Kbytes

6) MPEG Process & Video Encoder Process Start

STi5518 Encoder configured in PAL BGDHI
Mpeg audio/video synchro process started
Mpeg live reset process started
Setting up the mpeg video interrupt
5518 initialized to parse PES streams
Setting up the mpeg audio interrupt

7) Teletext Driver & Process Start

```
Teletext driver library v1.0 - Version of Apr 04 2000 at 01:34:03
Creating 'Teletext VBI task' (priority=9)
The 'teletext_data_transfer' task is running
Creating 'Teletext STB Page Filter' task (priority=9)
The 'ttx_stb_page_filter' task is running
Creating 'Teletext Handler' task (priority=9)
'teletext_handler' task is running
```

8) User Data Loading & Save

```
load gpos.....read crc = 5da2a839 : write crc = 5da2a839
***
.....LOAD POSt -----> OK! ; serivce_num = 0
*****
.....LOAD POSt parsing process start ************
.....LOAD POSt parsing process start ************
.....LOAD POSt parsing process start ************
.....LOAD POSt parsing process start ************
.....LOAD POSt parsing process start ************
......Last Channel didn't save before !!!!
......Last Channel didn't save before !!!!
```

9) API Kernel Process Start

```
SMALLWIN smallwin_scheduler PROCESS STARTED .....
smallwin_scheduler start..... ok
```

10) Initializing AUDIO PES Manager

```
469 audiopes.c> Initialising AUDIO PES Manager ...
510 audiopes.c> AUDIO PES Manager is created successfuly ...
```

11) "OK" or "Fail" Message

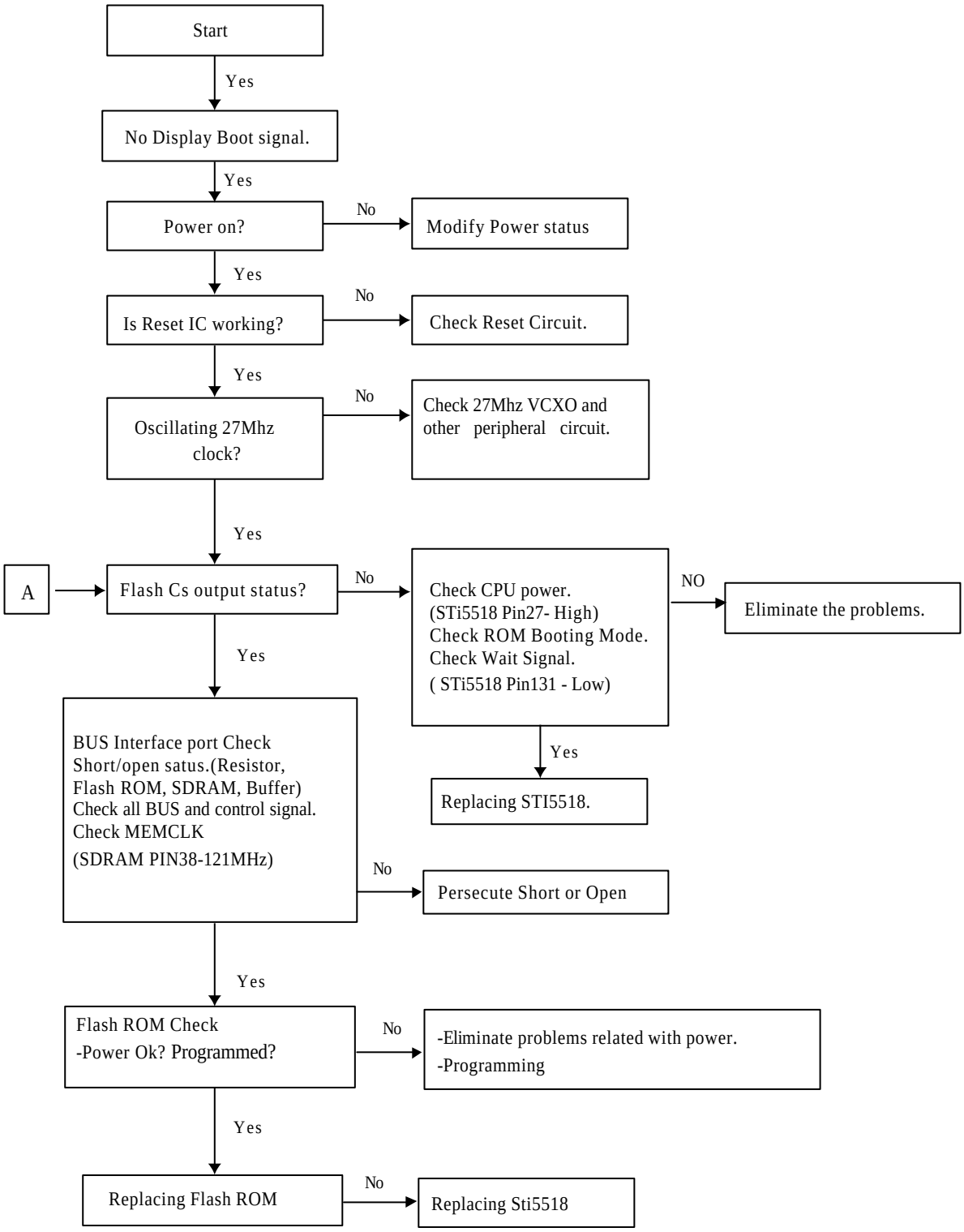
```
--[No errors during initialization !!!]--

-----------------------------------------
----------   OOO OO     O O      OO OOO ----------
----------   OO OO O    OO     O O OOO ----------
----------  OO       OO   OO   O O ----------
---------- OO          OO  OO O O ----------
---------- OO          OO  OOOO     ----------
---------- OO          OO  OO OO    ----------
---------- OO          OO  OO  OO   ----------
----------  OO       OO   OO   OO  ----------
----------   OOO OO      OO     OO OOOO ----------
-----------------------------------------
-----------------------------------------
```

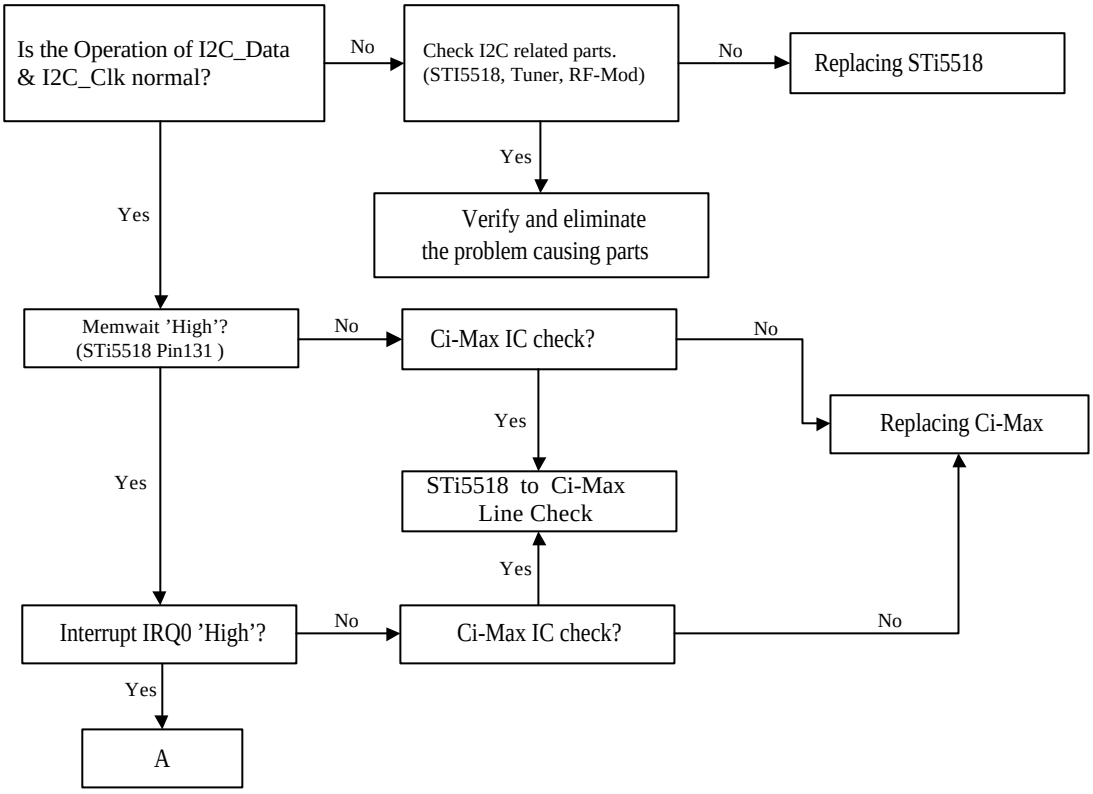
Ⅲ. FIXING ERRORS

1. BOOTING ERROR

(1) No response of Display Boot signal.

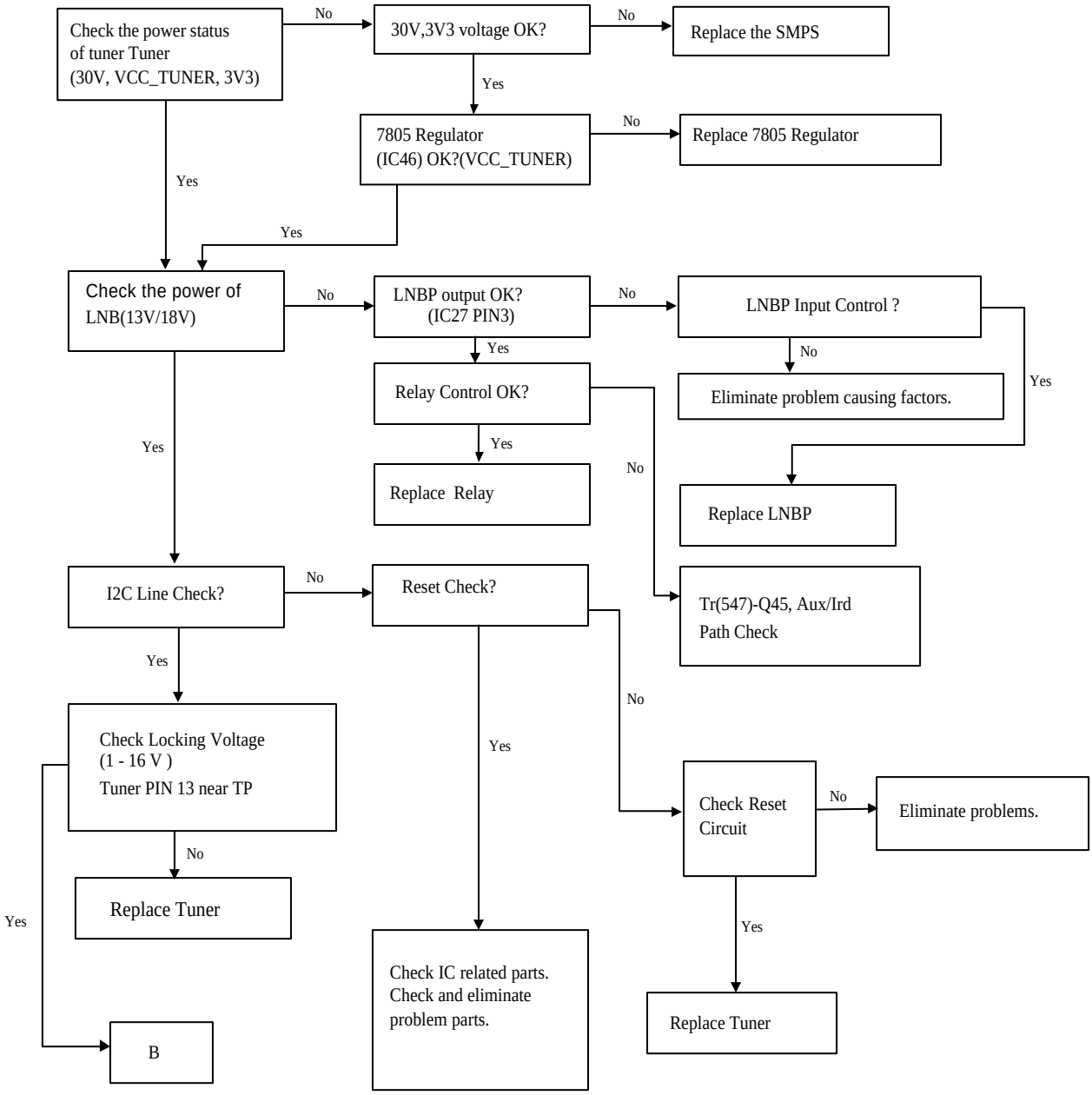


(2) Operation error after the BOOT signal

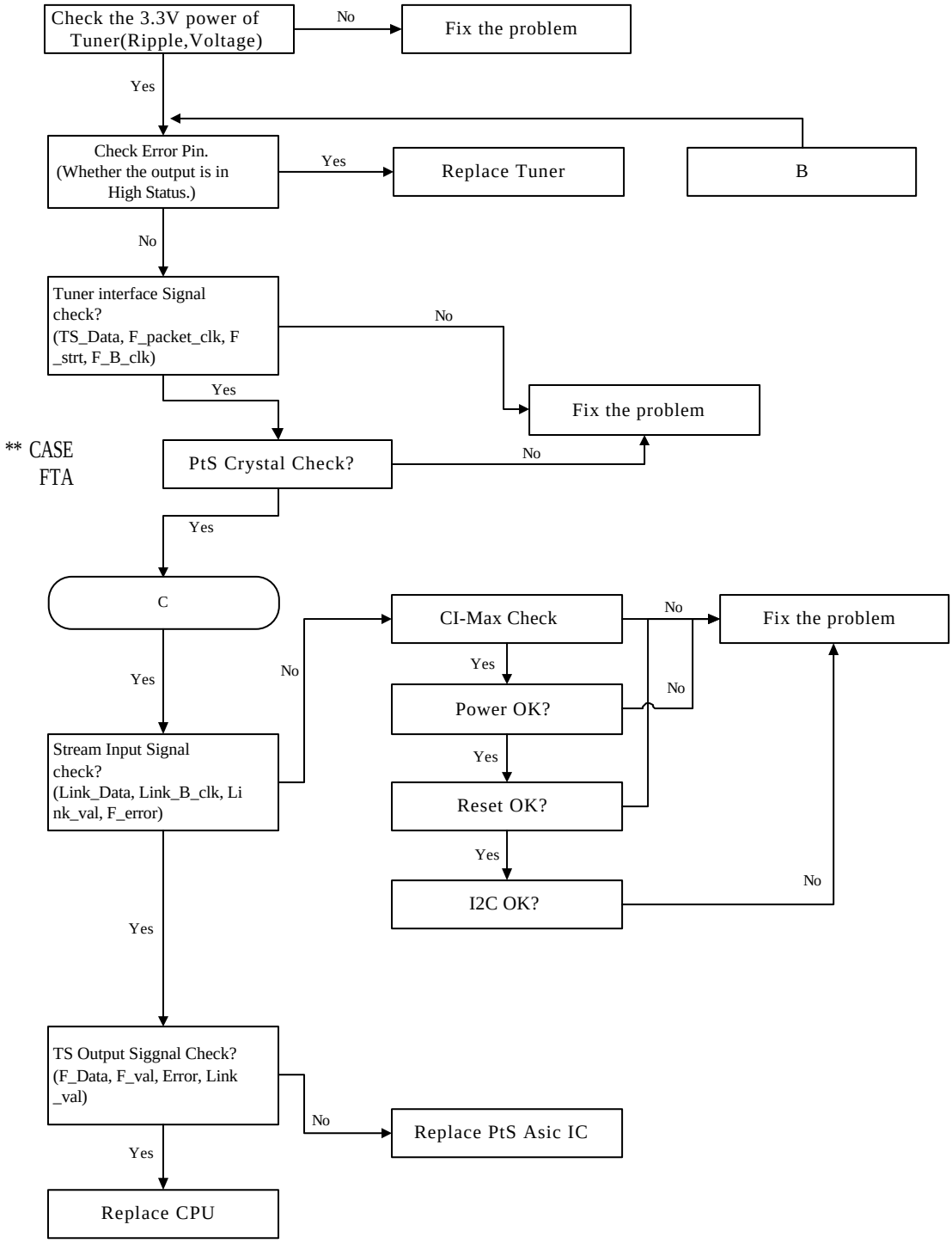


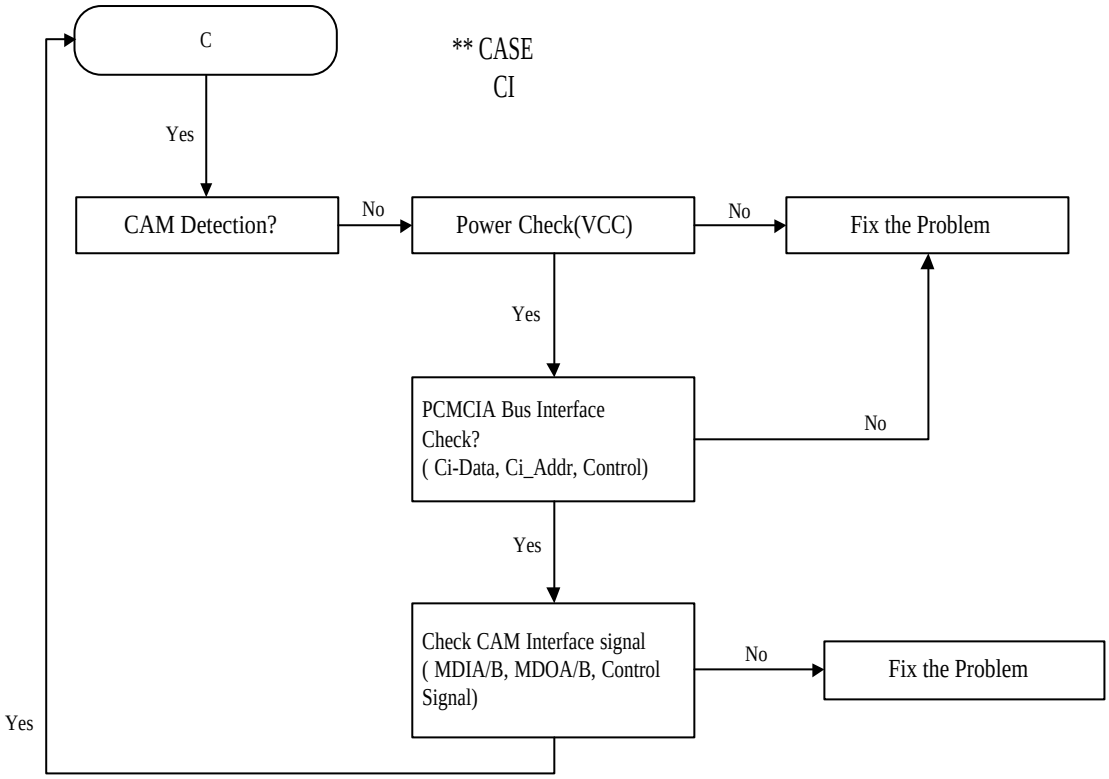
2. Poor quality screen

(1) Locking Error



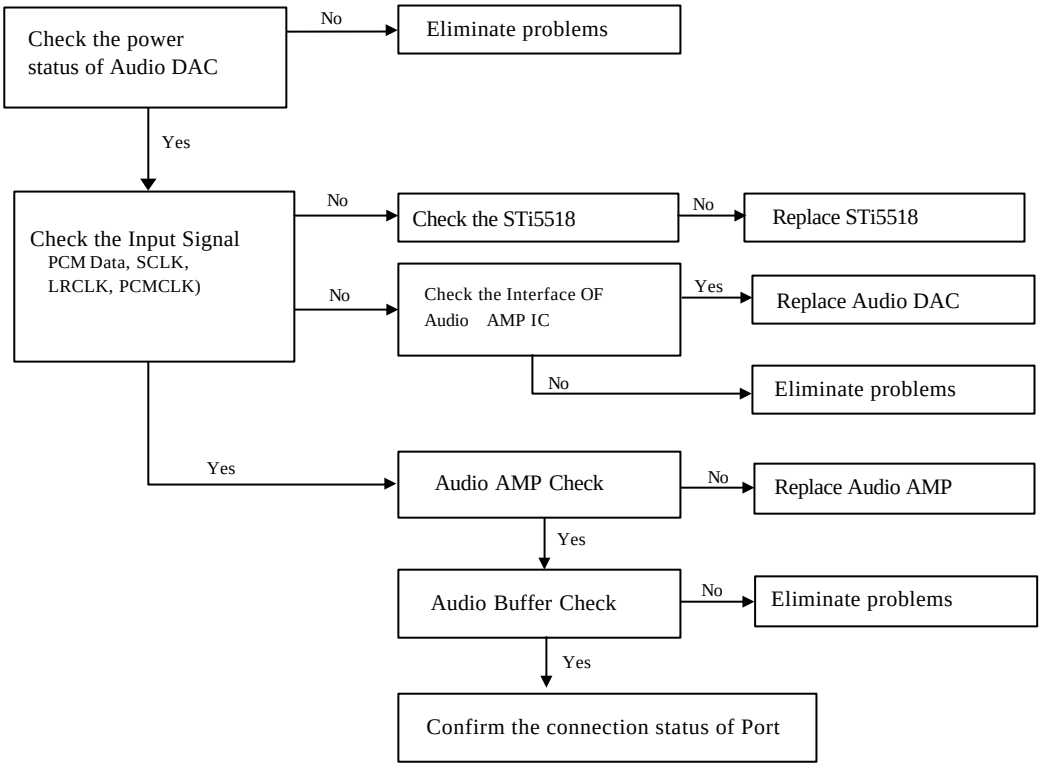
(2) Disabled screen after Locking



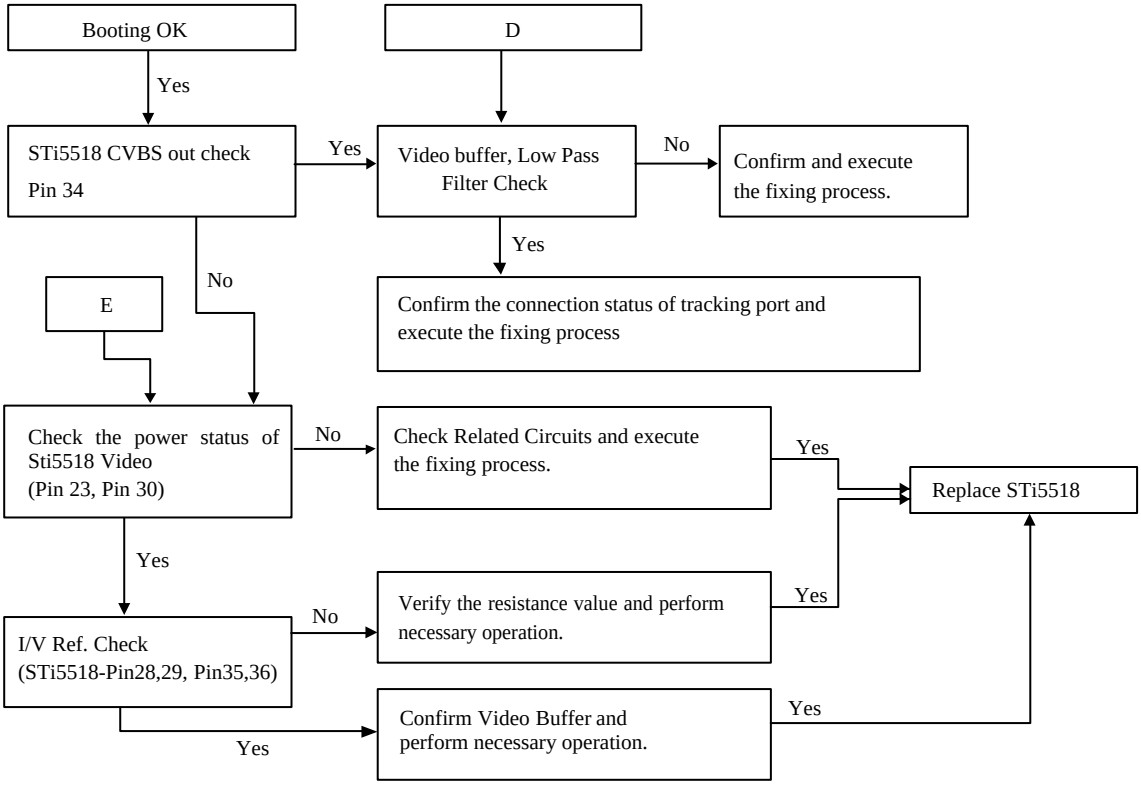

C
** CASE
CI
Yes
CAM Detection?
No
Power Check(VCC)
No
Fix the Problem
Yes
PCMCIA Bus Interface
Check?
(Ci-Data, Ci_Addr, Control)
No
Yes
Check CAM Interface signal
(MDIA/B, MDOA/B, Control
Signal)
No
Fix the Problem
Yes

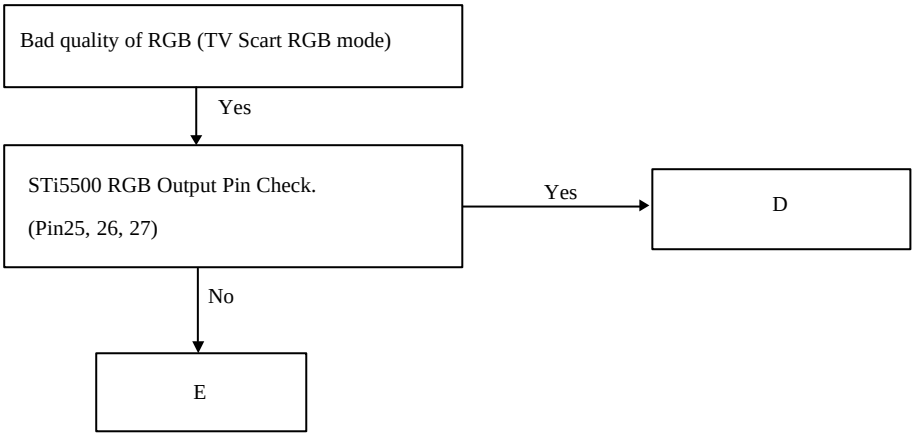
3. Errors in Audio and Video

(1) AUDIO ERROR



(2) VIDEO ERROR





NO	PART NAME MAIN PCB	DESCRIPTION	PART NAME	Q'TY	LOCATION NO. CI
1	C CHIP CERA	10pF, 50V,(±5%), Size : 1.6 * 0.8mm	C1608C0G1H100D	3	C21, C195,C248
2	C CHIP CERA	33pF,50V, (±5%), Size : 1.6 * 0.8mm	C1608C0G1H330J	16	C41,C42,C43,C44,C45,C46,C47,C48,C49,C50C51,C52,C53,C54,C55,C56
3	C CHIP CERA	150pF,50V,(±5%),Size : 1.6 * 0.8mm	C1608C0G1H151J	1	C206
4	C CHIP CERA	270pF,50V,(±5%),Size : 1.6 * 0.8mm	C1608C0G1H271J	9	C183,C184,C186,C188,C200,C201,C250,C252,C254
5	C CHIP CERA	390pF, 50V,(±5%), Size : 1.6 * 0.8mm	C1608C0G1H391J	20	C134,C135,C141,C142,C148,C149,C155,C156,C162,C163C169,C170,C211,C212,C216,C217,C222,C223,C237,C239
6	C CHIP CERA	1000pF,50V,(±5%),Size : 1.6 * 0.8mm	C1608X7R1H102J	2	C291,C292
7	C CHIP CERA	2.2nF, 50V,(±10%), Size : 1.6 * 0.8mm	C1608X7R1H222K	1	C300
8	C CHIP CERA	3.3nF, 50V,(±10%), Size : 1.6 * 0.8mm	C1608X7R1H332K	4	C133,C140,C147,C168
9	C CHIP CERA	3.9nF, 50V,(±10%), Size : 1.6 * 0.8mm	C1608X7R1H392K	5	C154,C161,C210,C221,C226
10	C CHIP CERA	10nF,50V,(±10%),Size : 1.6 * 0.8mm	C1608X7R1H103K	4	C81,C84,C87,C88
11	C CHIP CERA	22nF,50V,(±10%), Size : 1.6 * 0.8mm	C1608X7R1H223K	12	C1,C2,C4,C5,C7,C8,C10,C11,C13,C14C16,C17
12	C CHIP CERA	47nF,50V,(±10%), Size : 1.6 * 0.8mm	C1608X7R1E473K	1	C299
13	C CHIP CERA	0.1uF, 50V,(+80%~-20%), Size : 1.6 * 0.8mm	C1608Y5V1H104Z	79	C19,C20,C24,C28,C31,C60,C61,C70,C91,C92C93,C94,C95,C96,C97,C98,C99,C100, C101,C102C103,C104,C105,C106,C111,C112,C114C121,C122C123,C124,C125, C126,C136,C143,C150,C157,C164,C171C194,C205,C207,C213,C219,C225,C231, C233,C236,C243C256,C262,C264,C268,C270,C271,C278,C280,C283,C285C290, C294,C301,C302,C400,C401CX1,CX2,CX3,CX4,CX5,CX6,CX9,CX10,CX11CX17, CX18,CX22,CX23,CX80
14	C CHIP CERA	1uF,50V,(+80%~-20%),Size : 1.6 * 0.8mm	C1608Y5V1A105Z	1	C244
15	C ELECTRO	1uF, 50V, (±20%, Size: 5 * 11) RSS	CEXF1H109V	4	C273,C274,C275,C276
	C ELECTRO	4.7uF, 50V, (±20%, Size: 5 * 11) RSS	CEXF1H479V	4	C185,C187,C251,C253
16	C ELECTRO	10uF,25V (±20%, Size: 5 * 11) RSS	CEXF1E100V	18	C30,C89,C181,C182,C235,C238,C242C263,C269,C272,C277,C281,C286,C293,CX15,CX16,CX20,CX21
17	C ELECTRO	10uF,50V (±20%, Size: 5 * 11) RSS	CEXF1H100V	1	C282
18	C ELECTRO	22uF, 16V (±20%, Size: 5 * 11) RSS	CEXF1C220V	7	C198,C199,C204,C227,C228,C240,C241
19	C ELECTRO	22uF, 35V (±20%, Size: 5 * 11) RSS	CEXF1V220V	1	C303
20	C ELECTRO	22uF, 50V (±20%, Size: 5 * 11) RSS	CEXF1H220V	2	C15,C18
21	C ELECTRO	47uF, 16V (±20%, Size: 5 * 11) RSS	CEXF1C470V	7	C83,C131,C152,C159,C229,C215,C234
22	C ELECTRO	47uF, 35V (±20%, Size: 6.3 * 11) RSS	CEXF1V470V	1	C12
23	C ELECTRO	100uF, 16V (±20%, Size:6.3 * 11) RSS	CEXF1C101V	20	C23,C57,C82,C85,C110,C120,C132,C139,C146,C153,C160,C167,C197,C202C208,C220,C232,C255,C267,C289
24	C ELECTRO	100uF, 50V (±20%, Size: 8 * 11.5) RSS	CEXF1H101V	1	C261
25	C ELECTRO	220uF, 16V (±20%, Size: 8 * 11.5) RSS	CEXF1C221V	6	C3,C6,C9,C22,C25,C26
26	C ELECTRO	1000uF, 16V (±20%, Size: 10 * 20) RSS	CEXF1C102V	1	C86
27	R CHIP	1/10W,0 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		15	XR57,XR246,XR247,R264,R149,R150,R217,R222R26,RX80,RX81,RX83,RX84,RX85,RX87
28	R CHIP	1/10W,7.5 ohm,J±fi (±5%), Size : 1.6 * 0.8mm		3	R83,R91,R95
29	R CHIP	1/10W,8.2 ohm,J±fi (±5%), Size : 1.6 * 0.8mm		6	R103,R110,R130,R159,R163,R178

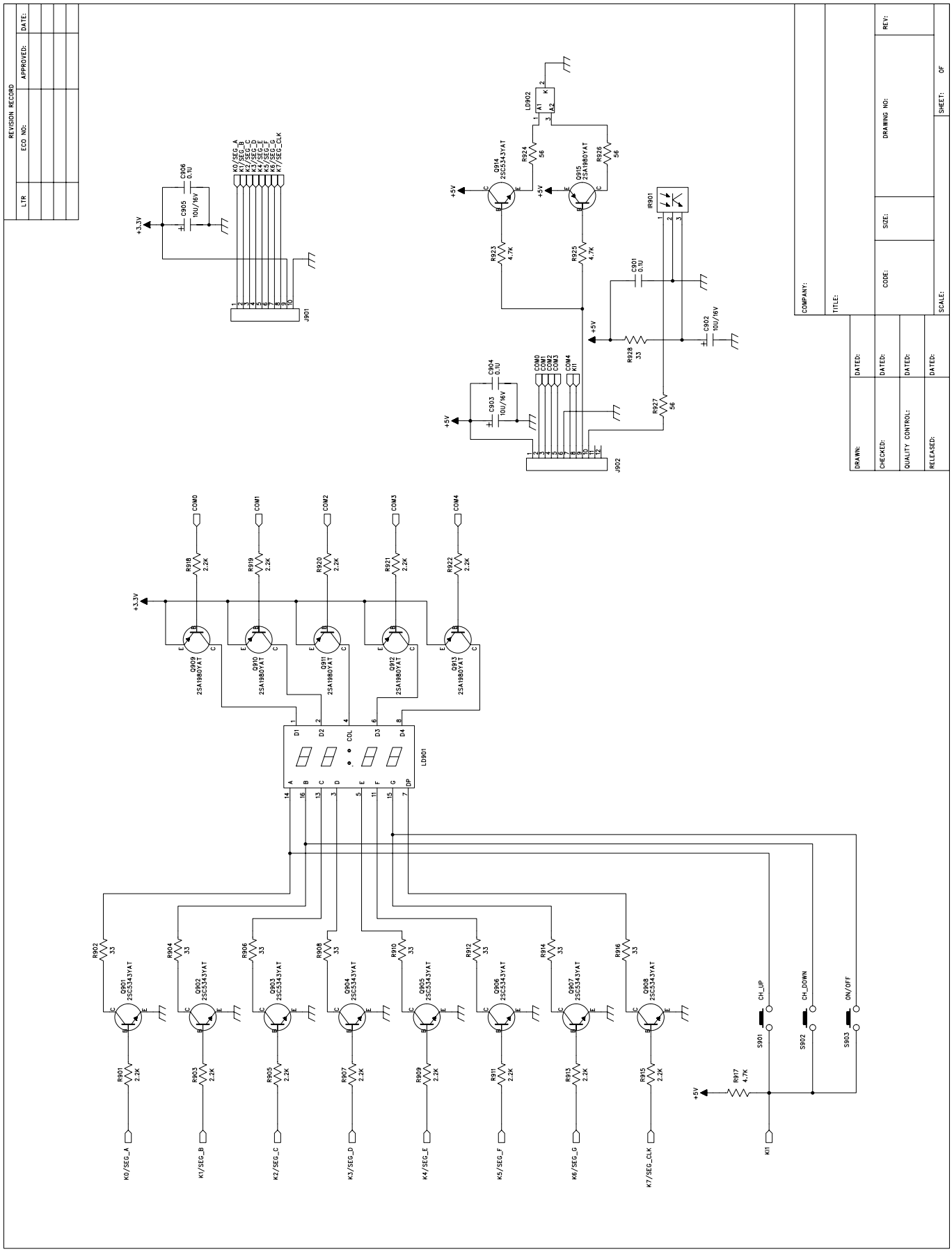
NO	PART NAME MAIN PCB	DESCRIPTION	PART NAME	Q'TY	LOCATION NO. CI
30	R CHIP	1/10W,10 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R276
31	R CHIP	1/10W,11 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R162
32	R CHIP	1/10W,12 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		7	R82,R90,R94,R109,R128,R158,R177
33	R CHIP	1/10W,13 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R102
34	R CHIP	1/10W,22 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		2	R14 ,R4
35	R CHIP	1/10W,33 ohm, J±fi (±5%), Size : 1.6 * 0.8mm		"27"	R10,R24,R197,R252,R261, R251,R253,R254,R255,R256,R257,R258 ,R259,R260,RX5RX6,RX8,RX9,RX10,RX11,RX12,RX13,RX14,RX15,RX17RX18,RX19
36	R CHIP	1/10W, 56 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		"8"	R7,R25,R191,R192,R193,R194RX7,RX16"
37	R CHIP	1/10W,75 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		14	R86,R92,R98,R104,R108,R131,R161,R164,R165,R171R174,R176,R179,R185
39	R CHIP	1/10W,200 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		2	R126,R273
40	R CHIP	1/10W,220 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		4	R84,R88,R96,R100
41	R CHIP	1/10W,240 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R275
42	R CHIP	1/10W,270 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R172
43	R CHIP	1/10W,330 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R106
43	R CHIP	1/10W,470 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R156
45	R CHIP	1/10W,680 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		4	R141,R142,R166,R167
46	R CHIP	1/10W,820 ohm, J±fi (±5%) Size : 1.6 * 0.8mm		8	R81,R87,R93,R99,R105,R111,R157,R173
47	R CHIP	1/10W,1K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		16	R36,R145,R147,R152,R183,R184,R186,R211R215,R220,R232,R233,R238,R266,RX32,RX33
48	R CHIP	1/10W,2.2K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		12	R85,R89,R97,R101,R107,R129,R160,R175R199,R202,RX88,RX89
49	R CHIP	1/10W,3K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R270
50	R CHIP	1/10W,3.3K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R274
51	R CHIP	1/10W,4.7K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		5	R6,R210,R265,R22,R23
52	R CHIP	1/10W,5.6K ohm,J±fi (±5%) Size : 1.6 * 0.8mm		1	R269
53	R CHIP	1/10W,6.8K ohm,J±fi (±5%) Size : 1.6 * 0.8mm		2	R200,R203
54	R CHIP	1/10W,7.5K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R278
55	R CHIP	1/10W,8.2K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R169
56	R CHIP	1/10W,10K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		33	R1,R11,R12,R13,R27,R28,R31,R32R33,R34,R35,R61,R71,R72,R170,R181,R182R240,R241,R271,R234,R235, R400,R401RX1,RX2,RX3,RX4,RX34,RX35,RX71,RX73,RX86
57	R CHIP	1/10W,12K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R151
58	R CHIP	1/10W,15K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		3	R29,R30,R272
59	R CHIP	1/10W,18K ohm, J±fi (±5%) Size : 1.6 * 0.8mm		1	R168
60	R CHIP	1/10W,22K ohm, J±fi(±5%),Size : 1.6 * 0.8mm		9	R201,R204,R205,R206,R213,R218,R268,R277,R279
61	R CHIP	1/10W,39K ohm, J±fi(±5%),Size : 1.6 * 0.8mm		3	R214,R219,R237
62	R CHIP	1/10W,47K ohm, J±fi(±5%),Size : 1.6 * 0.8mm		6	R38,R209,R212,R231,R236,R267
63	R CHIP	1/10W,100K ohm,J±fi (±5%) Size : 1.6 * 0.8mm		7	R143,R144,R146,R148,R216,R221,R239

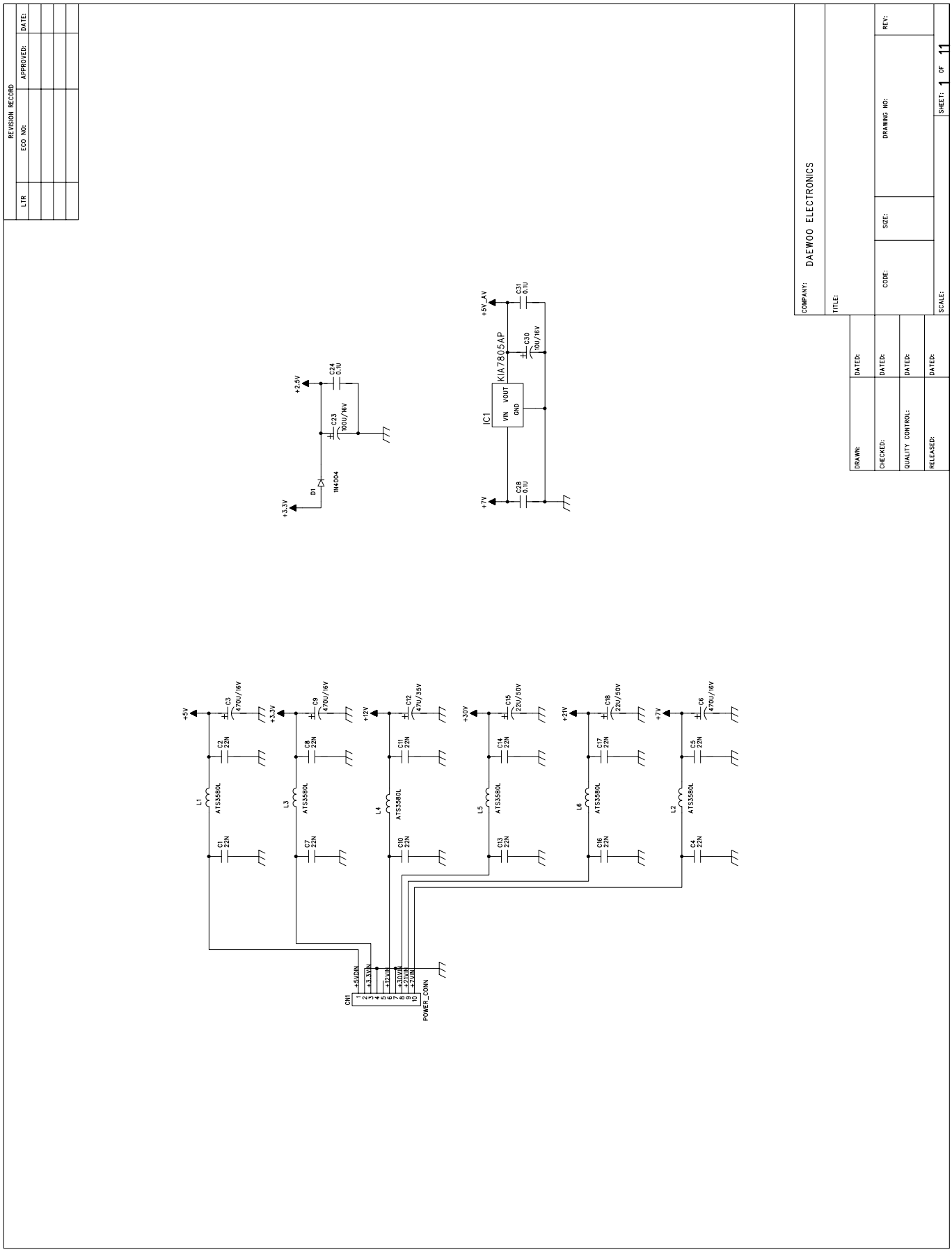
NO	PART NAME MAIN PCB	DESCRIPTION	PART NAME	Q'TY	LOCATION NO. CI
64	R METAL FILM	Axial, 470ohm, MOF 2W, ±5%, SAMLL	2W,470 ohm,J,SMALL	1	R262
65	R CARBON FILM	Axial, 560ohm, Carbon Film, 1/4w, ±5%	"1/4,560 OHM,J"	1	R180
66	R CHIP ARRAY	CHIP ARAY, 33 ohm J 3.2 * 1.6mm	CN1J4ATD330J	31	MNR1,MNR2,MNR3,MNR5,MNR6,MNR7,MNR8MNR9,MNR10,MNR12,MNR13,MNR14, MNR15MNR16MNR17,MNR18,MNR19,MNR20,MNR21,MNR23,MNR24RPX1,RPX2,RPX3, RPX4,RPX20,RPX21,RPX70,RPX71,RPX80,RPX81
67	L CHIP MULTI	CHIP, 120 uH, SMD (±10%), Size : 2.0 * 1.2mm	WB201209B121KNT	17	L7,L15.L19,L21,L28,L30,L41,L43,L45,L52L61,L62LX1,LX2,LX3,LX4,LX5
68	COIL BEAD	Axial, CHOKE COIL	ATS3580L(TP)	6	L1,L2,L3,L4,L5,L6
69	COIL PEAKING	2.7uH, K , RADIAL	5CPX279K—	9	L22,L24,L26,L29,L31,L33,L42,L44,L46
70	COIL PEAKING	22uH, J , RADIAL	5CPX220J—	1	L17
71	L CHIP	MLF,CHIP,10uH, ±5%, Size : 2.0 * 1.2mm		2	BL16,BL18
72	CHIP DIODE	1N4004S		1	D1
73	CHIP DIODE	ES1J		1	D20
74	DIODE CHIP	Melf Type, Switching Diode	LS4148	1	D5
75	TR CHIP	PNP, SOT-23, High speed Switching	SBT2907AF(2F)	10	Q11,Q12,Q13,Q14,Q15,Q16,Q21,Q23,Q24,Q25
76	TR CHIP	PNP, SOT-23, Switching Application	2SA1981SFY	1	Q44
77	TR CHIP	PNP, SOT-23, Switching Application	2SA1980SF (CAY)	3	Q26,Q40,Q46
78	TR CHIP	NPN, SOT-23, Switching Application	2SC5343SF (DAY)	16	Q20,Q22,Q27,Q28,Q29,Q30,Q31,Q35,Q36Q37,Q41,Q42,Q45,Q47,Q48,Q49
	TR	Audio power Amplifier, PNP, High current = -2A	STB1277YAT	1	Q77
	TR CHIP	KTA1663-Y-RTF , PNP	KTA1663	2	Q1,Q2
79	TR CHIP	KRC111S-RTK , NPN	KRC111S	2	Q3,Q4
80	IC CHIP	TTL (74HC04D), SMD TYPE	74HC04D	2	IC4,IC7
81	IC CHIP	TTL (74HC08D), SMD TYPE	74HC08D	1	IC6
82	IC CHIP	TTL (74HC32D), SMD TYPE	74HC32D	1	IC8
83	IC CHIP LOGIC	TTL (74HC138D), SMD TYPE	74HC138D	1	IC23
84	IC CHIP	TTL (74HC574D), SMD TYPE	74HC574D	1	IC24
85	IC CHIP	Low-cost stereo filter DAC	UDA1330ATS	1	IC25B
86	IC CHIP AV	VIDEO Switch	MM1232XFBE	1	IC22
87	IC CHIP	CHIP SET FOR DVB	STI5518BVB	1	IC14
88	IC CHIP DRIVE	RS232 Interface IC	SP232ACN	1	IC29
89	IC CHIP FL ASH MEMORY	FLASh Memory, 512K X 16BIT(1M BYTE), TSOP	MBM29LV800TA-90PFTN	1	IC18
90	IC CHIP SDRAM	SDRAM, 4M X 16BIT. 125MHZ, TSOP	HY57V641620HGT-H	1	IC21
91	IC REGULATOR	Voltage Regulator, Out Voltage=5V, TO-220	KIA7805AP	1	IC1
92	IC REGULATOR	Voltage Regulator, TO-220	KA317	1	IC33
93	IC CHIP AUDIO AMP	Audio Amp	KA358D	1	IC26
94	IC CHIP RESET	RESET IC (Voltage Detector=2.5V), SOT-89	ELM9725NAA	1	IC5

NO	PART NAME MAIN PCB	DESCRIPTION	PART NAME	Q'TY	LOCATION NO. CI
95	CRYSTAL OSCILATOR	27 MHz, 3.3V , FULL, 25PPM	4P,27.000000MHZ,25PPM"	1	VCXO
96	SW POLY	Poly Switch	RXE065-2	1	SW1
97	TUNER DBS	950~2150MHZ, Loop Through, DVB-S용,0IF	TDQF-S001F	1	TN1
98	MODULE RF	RF Modulator (PLL TYPE)	TAMC-G008D	1	MOD1
99	JACK MINI DIN JACK	DUAE-9619, SVHS Conn. Mini Din Socket 4Pin	DUAE-9619	1	CN3
100	CONNECTOR SCART	Scart Connector 42Pin, Shield Type	2203-42ST(B)	1	CN7
101	JACK RCA	CA JACK Conn.4PIN	2000-04-T	1	CN8
102	CONN D-SUB	D-Sub 9Pin RS-232C connector, 나사체결한 상태	3302-09P-AFS-G0-T	1	CN12
103	CONN WAFER	HEADER 1x10 , 3.96mm Pitch, POWER CONN.	PCS-1-10-F396-00	1	CN1
104	CONN WAFER	I-HEADER Pin 2x10 , 2.54mm Pitch	2110-DS20G(2.54)	1	CN2
105	CONN WAFER	WAFER Header 1x12P, STRAIT TYPE, 2.54mm Pitch	YW025-12	1	J1A
106	CONN WAFER	WAFER Header 1x10P, STRAIT TYPE, 2.54mm Pitch	YW025-10	1	J1
107	PCB MAIN	FR-4, 2LAYER, 330*246,D1B	DSD9250_MAIN	1	A001
108	POWER SUPPLY	DWPS-10	DWPS-10	1	MPS01
109	TRANSMITTER REMOCON	31KEY (38KHz)	R-44DS01	1	
110	CORD POWER AS	Power Cord, 220AC, 1.89m	KKP419C+BL102NG+TUBE=2100	1	PW01
111	SW POWER	POWER SWITCH ASS'Y, 110mm	KRA-1101+H03VVH2-F=110	1	PS01
113	R CHIP ARRAY	CHIP ARAY, 56 ohm J 3.2 * 1.6mm		8	RPX30,RPX31,RPX40,RPX41,RPX50,RPX51,RPX60,RPX61
114	IC CHIP	TTL (74LVC245AD), SMD TYPE	74LVC245AD	1	ICX4
115	IC CHIP	TTL (74LVC373AD), SMD TYPE	74LVC373AD	2	ICX2,ICX3
116	IC CHIP	CI controller IC	CIMAX 2.0	1	ICX1
	PCMCIA	PCMCIA SLOT	007222TF40A	1	PX1

NO	PART NAME FRONT PCB	DESCRIPTION	PART NAME	Q'TY	REFERENCE
	FRONT PCB				
1	PCB Front	FR-1, 1Layer 246*199(1 UNIT), (4연배),D1B	DSD9250_FRONT	1	A001
2	TR	PNP, General Small Signal Amplifier, TO-92	2SA1980-YAT	6	Q909,Q910,Q911,Q912,Q913,Q915
3	TR	NPN, General Small Signal Amplifier, TO-92	2SC5343-YAT	9	Q901,Q902,Q903,Q904,Q905,Q906,Q907,Q908,Q914
4	R CARBON FILM	Axial, Carbon Film 33 ohm, 1/6W, ±5%	RD-AZ330J	9	R902,R904,R906,R908,R910,R912,R914,R916,R928
5	R CARBON FILM	Axial, Carbon Film 56 ohm, 1/6W, ±5%	RD-AZ560J	3	R924,R926,R927
6	R CARBON FILM	Axial, Carbon Film 2.2K ohm, 1/6W, ±5%	RD-AZ222J	13	R901,R903,R905,R907,R909,R911,R913,R915,R918,R919R920,R921,R922
7	R CARBON FILM	Axial, Carbon Film 4.7K ohm, 1/6W, ±5%	RD-AZ472J	3	R917,R923,R925
8	C CERA	HIBK 50V,Axial 0.1uF, (±10%)	UP050F104Z	3	C901,C904,C906
9	C ELECTRO	ELEC. 10uF,16V , Size: 4* 7, RSS	CEXF1C100A	3	C902,C903,C905
10	LED DISPALY	Seven-Segment LED Display,0.4 inch,4Digit,Forming	LTC-4627G-01	1	LD901
11	LED	DUAL COLOR LED LAMP, F5mm	SAM5270	1	LD902
12	MODULE IR Receiver	Remote Control Receiver Module,38KHz,Forming	KSM-603TH2	1	IR901
15	CABLE AS	Flat Cable & Conn, 10Pin, 190mm, 2.5mm, 2mm Pitch	YH025-10+YBAT200-10ULW190	1	J901
16	CABLE AS	Flat Cable & Conn, 12Pin, 190mm, 2.5mm, 2mm Pitch	YH025-12+YBAT200-12ULW190	1	J902
17	SW TACT	Push-Down Tact Switch (5mm)	THVV502GDA	3	S901,S902,S903
	WIRE COFFER	AWG22 1/0.65 TIN COAT		0.55	JP1
	WIRE COFFER	AWG22 1/0.65 TIN COAT		0.55	JP902

V. SCHEMATIC DIAGRAM

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APPROVED:
DATE:
COMPANY: DAEWOO ELECTRONICS
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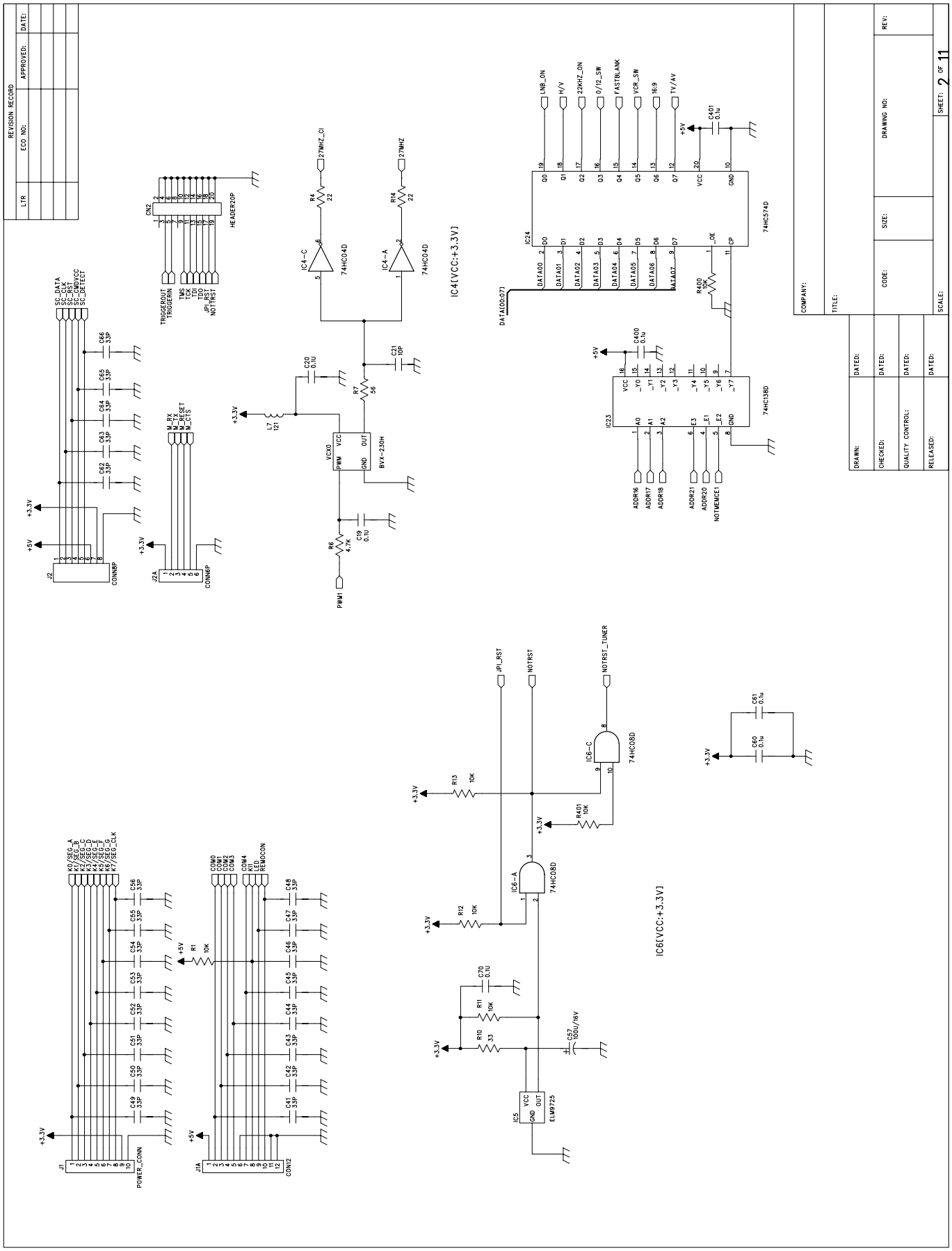
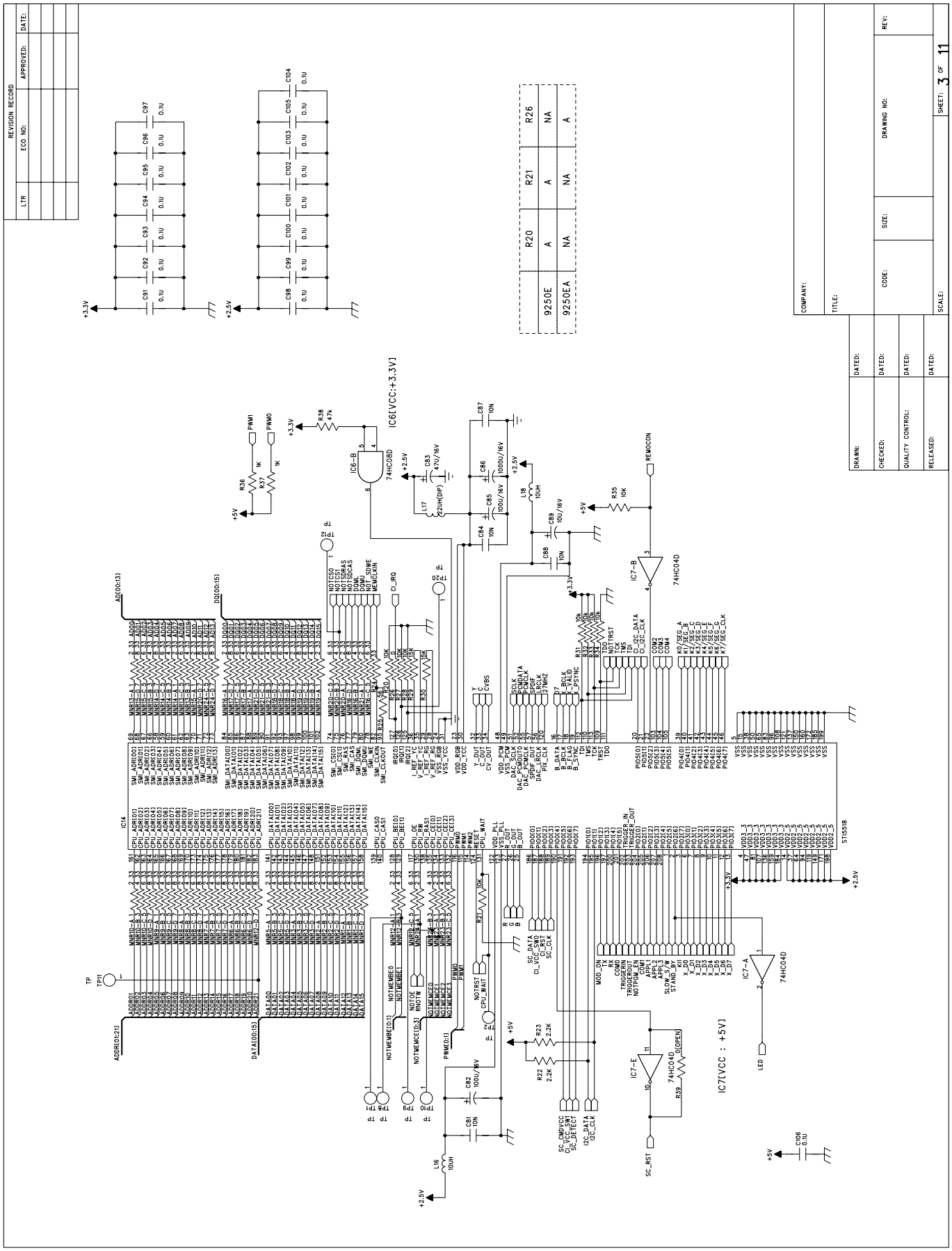
QUALITY CONTROL:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 1 OF 11
+2.5V
C24 0.1U
C23 100U/16V
D1 IN4004
+3.3V
IC1 KIA7805AP VIN VOUT GND
+5V_AV
C31 0.1U
C30 100U/16V
C28 0.1U
+7V
+5V
+3.3V
+12V
+30V
+21V
+7V
C3 470U/16V
C9 470U/16V
C12 47U/35V
C15 22U/50V
C18 22U/50V
C6 470U/16V
C2 22N
C8 22N
C11 22N
C14 22N
C17 22N
C5 22N
C1 22N
C7 22N
C10 22N
C13 22N
C16 22N
C4 22N
L1 ATS3580L
L3 ATS3580L
L4 ATS3580L
L5 ATS3580L
L6 ATS3580L
L2 ATS3580L
CN1
+5VDIN
+3.3VDIN
+12VDIN
+30VDIN
+21VDIN
+7VDIN
POWER_CONN

SCHEMATIC DIAGRAM





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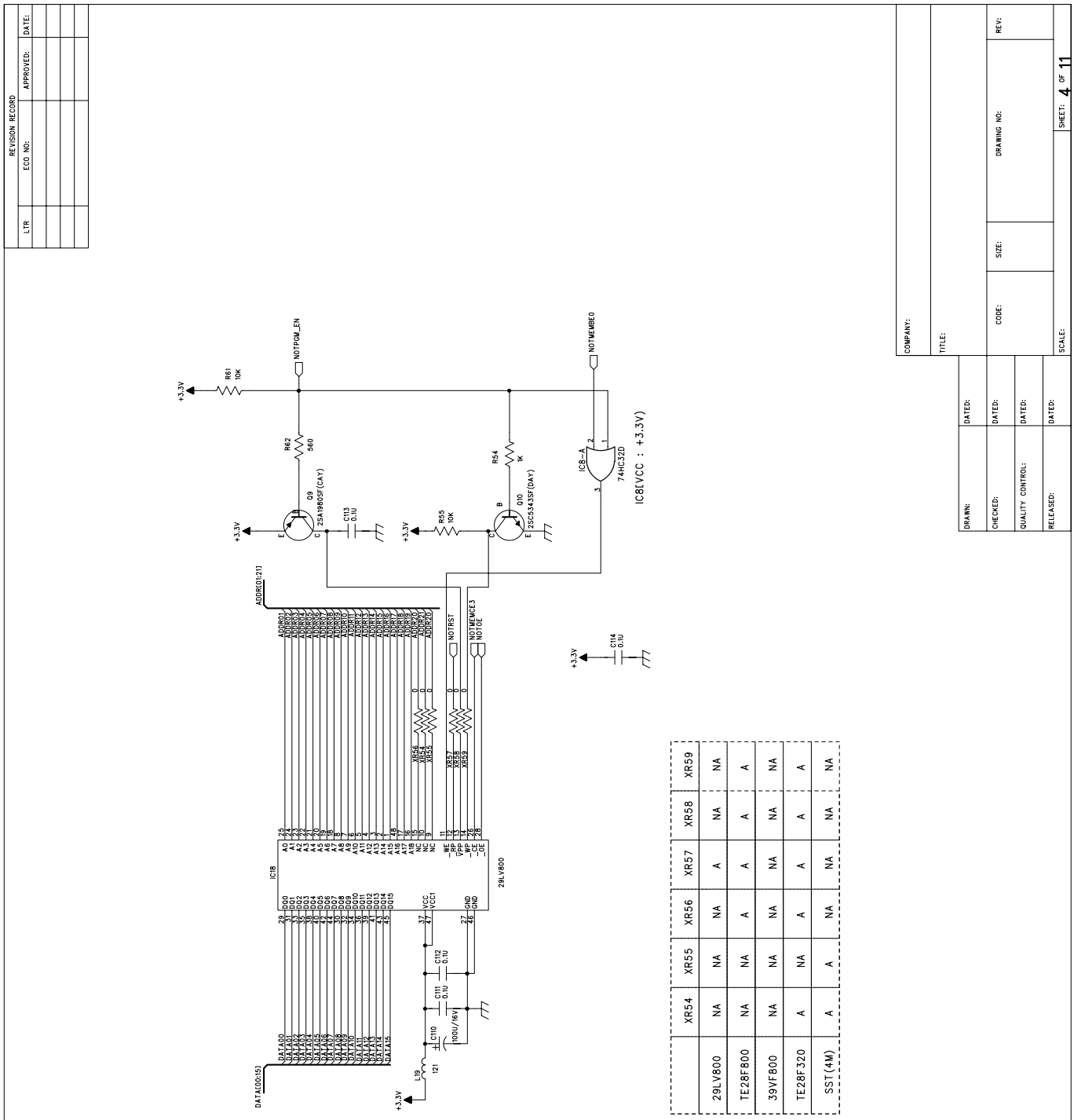
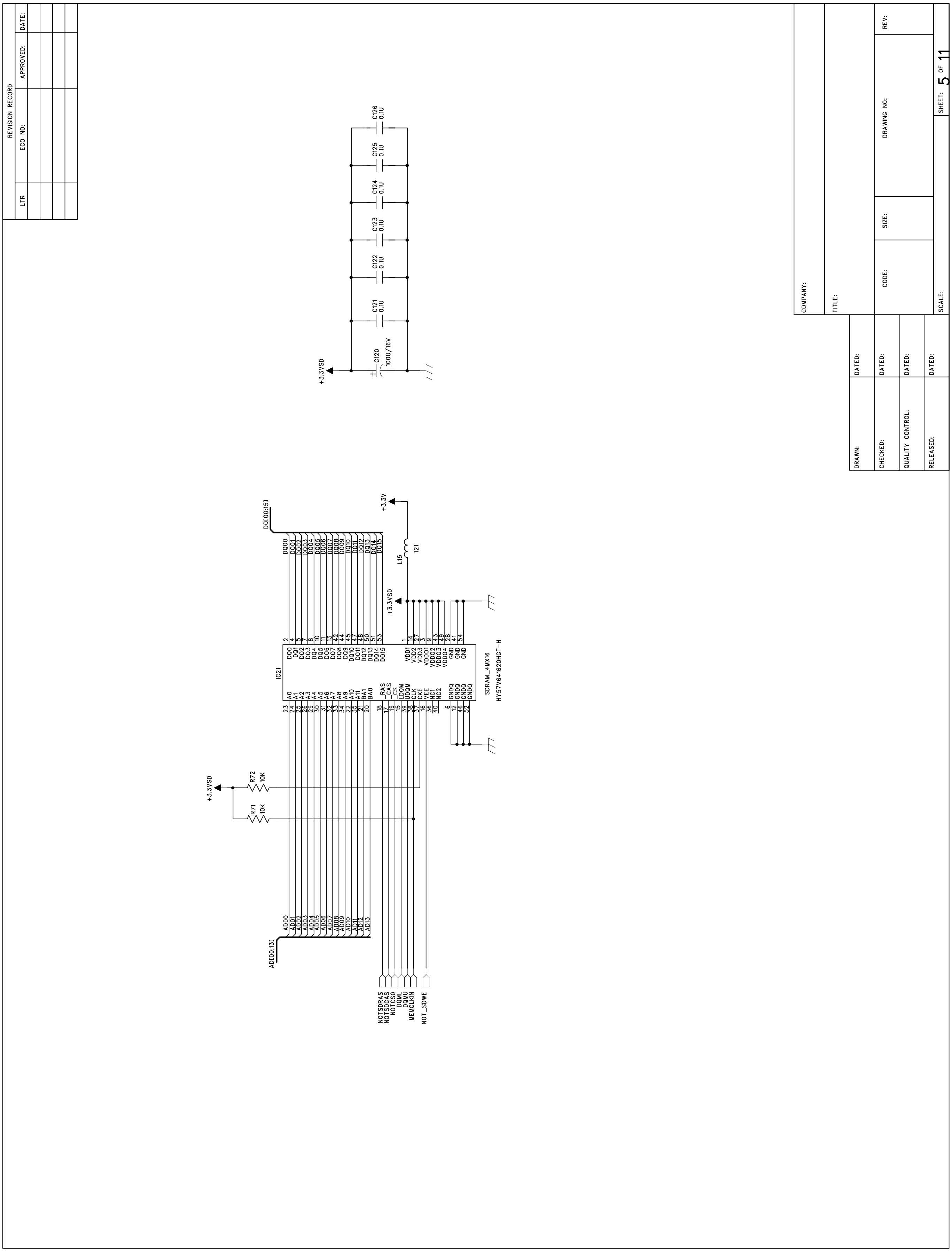


	XR54	XR55	XR56	XR57	XR58	XR59
29LV800	NA	NA	NA	A	NA	NA
TE28F800	NA	NA	A	A	A	A
39VF800	NA	NA	NA	NA	NA	NA
TE28F320	A	NA	A	A	A	A
SST(4M)	A	A	NA	NA	NA	NA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CHECKED:
QUALITY CONTROL:
RELEASED:
C120 100U/16V
C121 0.1U
C122 0.1U
C123 0.1U
C124 0.1U
C125 0.1U
C126 0.1U
+3.3VSD
+3.3V
L15
121
DQ[00:15]
AD[00:13]
IC21
SDRAM_4MX16
HY57V641620HGT-H
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R72 10K
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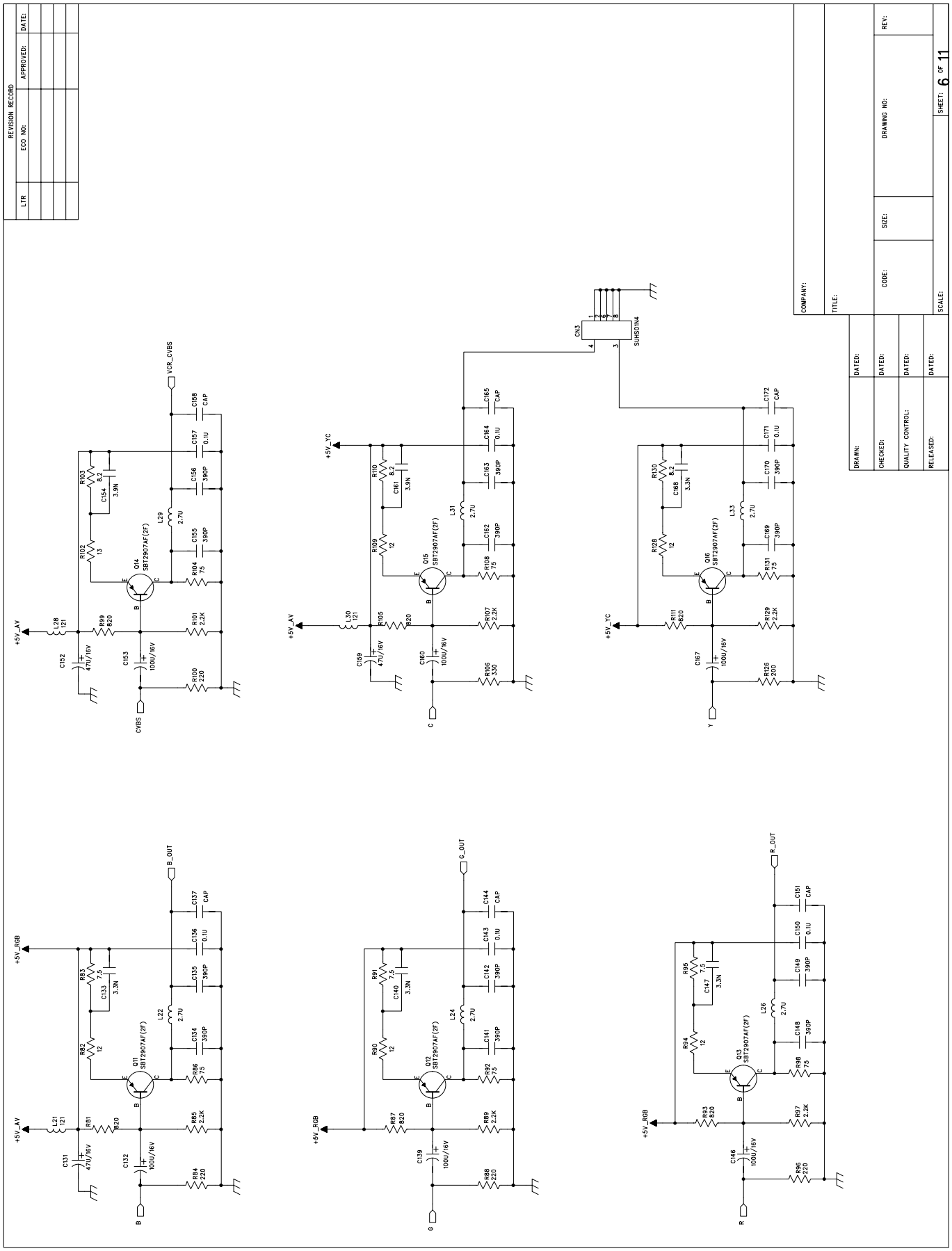
DQMU
MEMCLKIN
NOT_SDWE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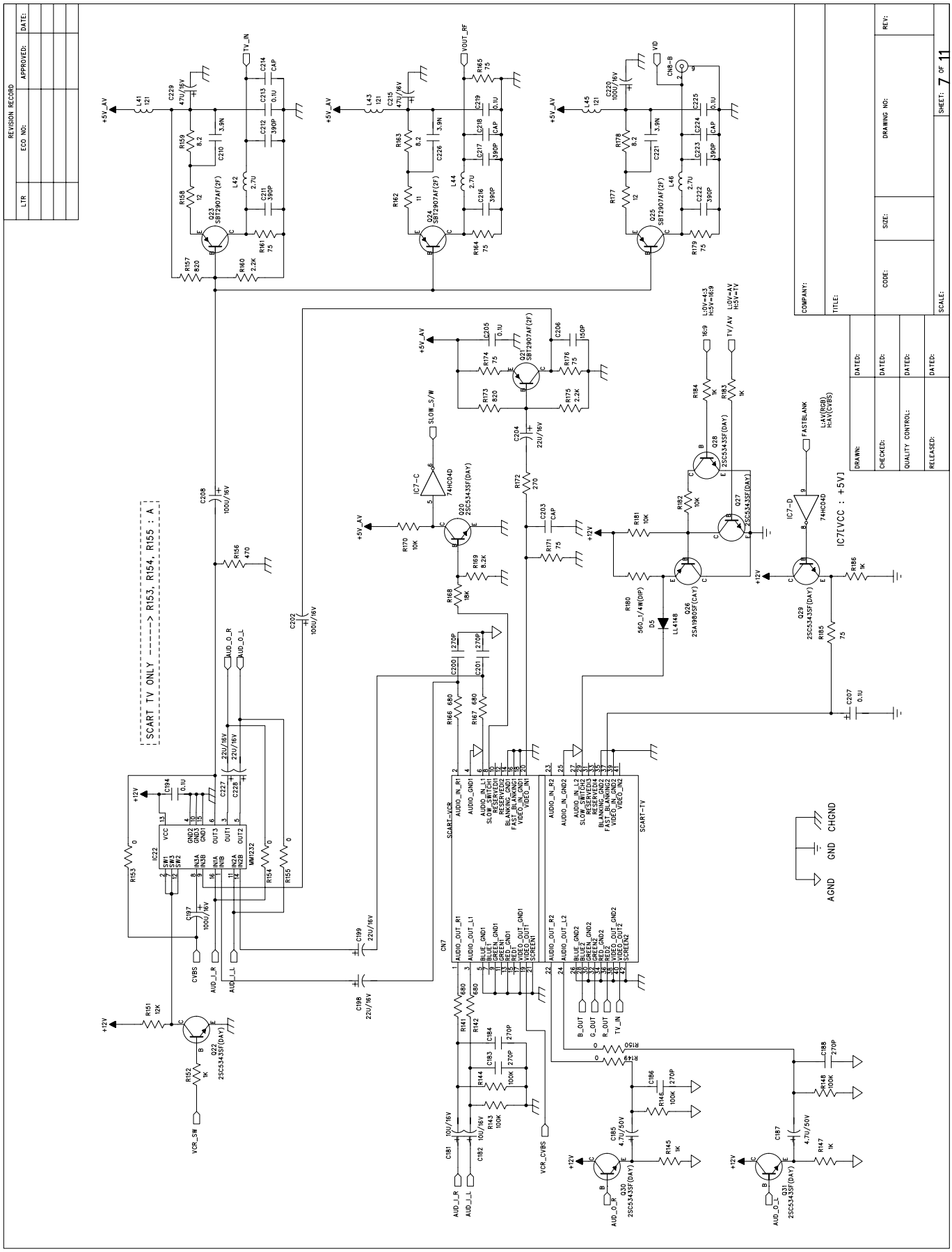
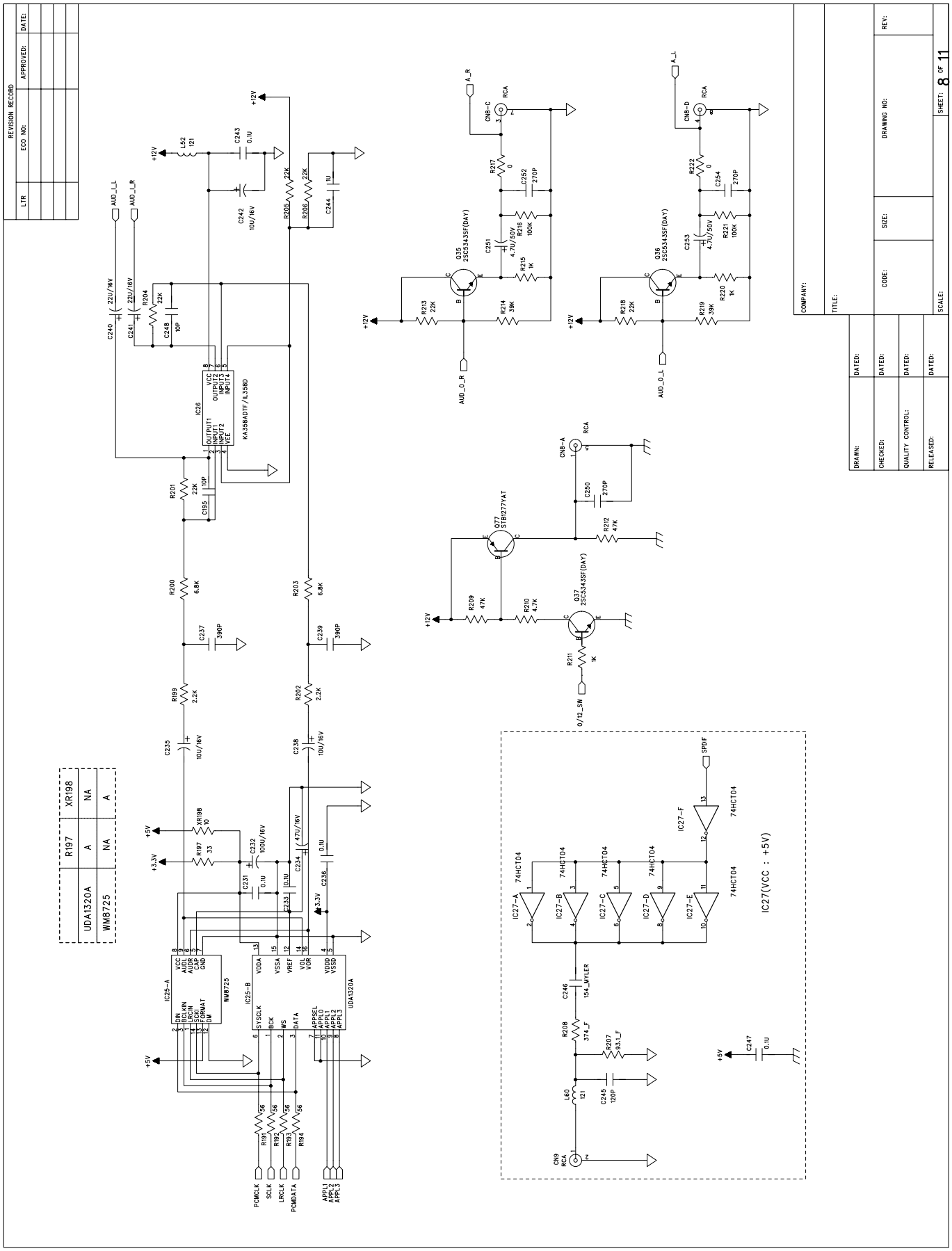
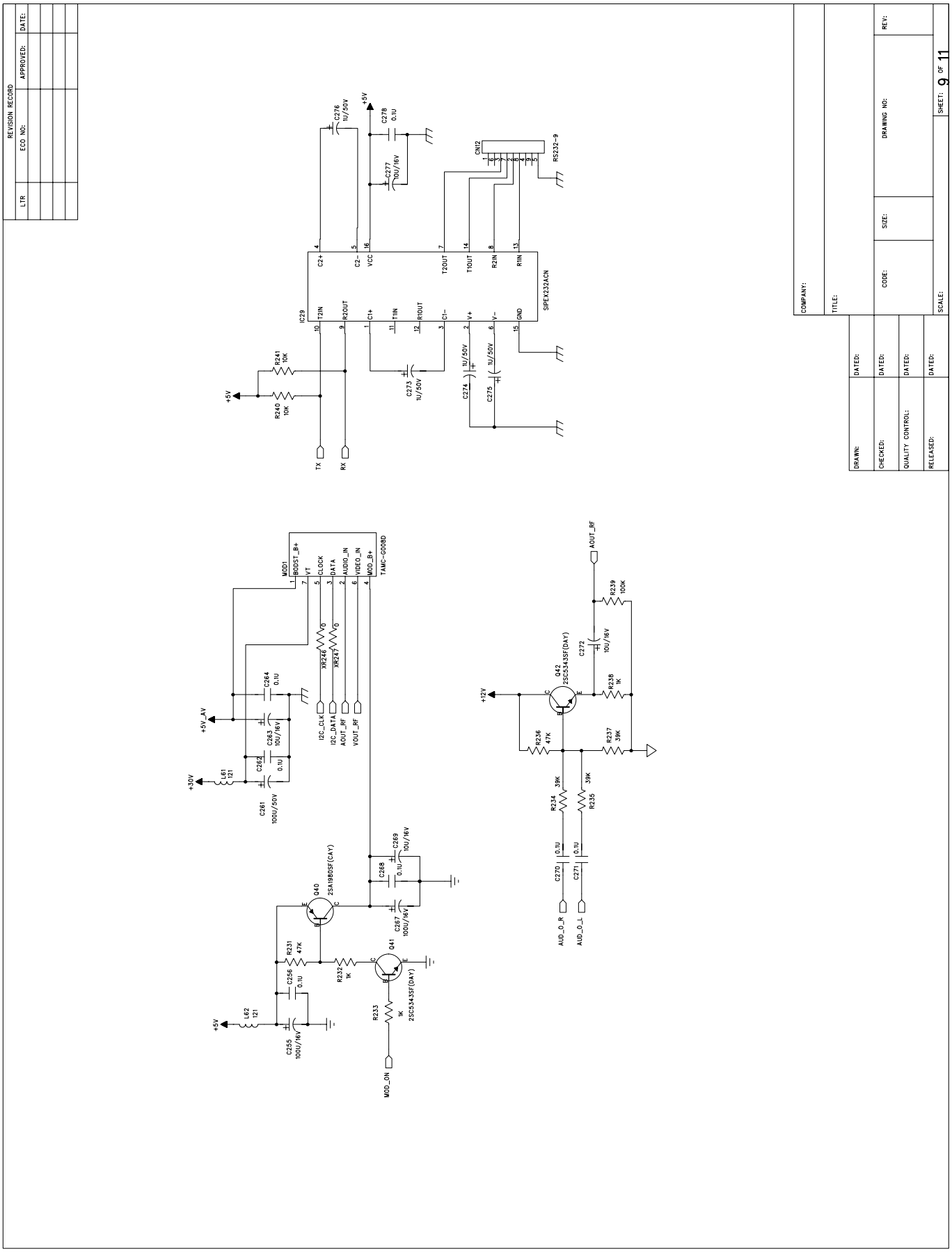
DATED:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 6 OF 11
VCR_CVBS
CVBS
+5V_AV
Q14 SBT2907AF(2F)
Q15 SBT2907AF(2F)
Q16 SBT2907AF(2F)
CN3
SUHSDIN4
+5V_YC
C
Y
B_OUT
G_OUT
R_OUT
+5V_RGB
Q11 SBT2907AF(2F)
Q12 SBT2907AF(2F)
Q13 SBT2907AF(2F)
B
G
R


SCART TV ONLY ----> R153, R154, R155 : A
IC7[VCC : +5V]
AGND GND CHGND

SCHEMATIC DIAGRAM

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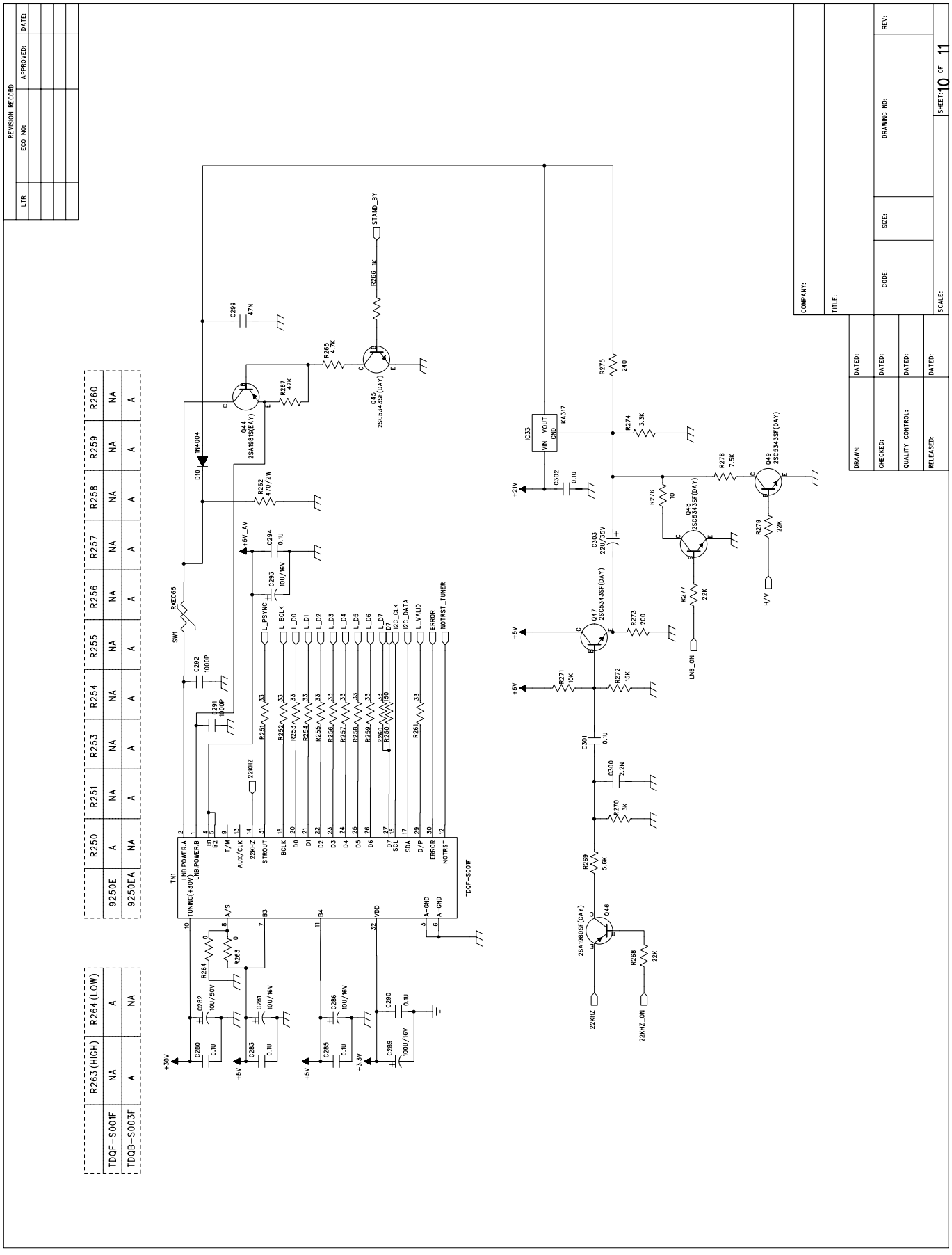
RELEASED:
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 9 OF 11
IC29
SIPEX232AON
C2+
C2-
VCC
T2OUT
T1OUT
R2IN
R1IN
T2IN
R2OUT
C1+
T1IN
R1OUT
C1-
V+
V-
GND
C276 1U/50V
C278 0.1U
C277 10U/16V
C273 1U/50V
C274 1U/50V
C275 1U/50V
R241 10K
R240 10K
+5V
CN12
RS232-9
TX
RX
MOD1
TAMC-G008D
BDOST_B+
VT
CLOCK
DATA
AUDIO_IN
VIDEO_IN
MOD_B+
XR246
XR247
I2C_CLK
I2C_DATA
AOUT_RF
VOUT_RF
C264 0.1U
C263 10U/16V
C262 0.1U
C261 1000U/50V
+5V_AV
+30V
L61 121
Q40 2SA1980SF(CAY)
Q41 2SC5343SF(DAY)
C269 10U/16V
C268 0.1U
C267 100U/16V
R231 47K
R232 1K
R233 1K
C256 0.1U
C255 100U/16V
L62 121
MOD_ON
Q42 2SC5343SF(DAY)
+12V
AOUT_RF
R239 100K
C272 10U/16V
R238 1K
R236 47K
R237 39K
R234 39K
R235 39K
C270 0.1U
C271 0.1U
AUD_O_R
AUD_O_L

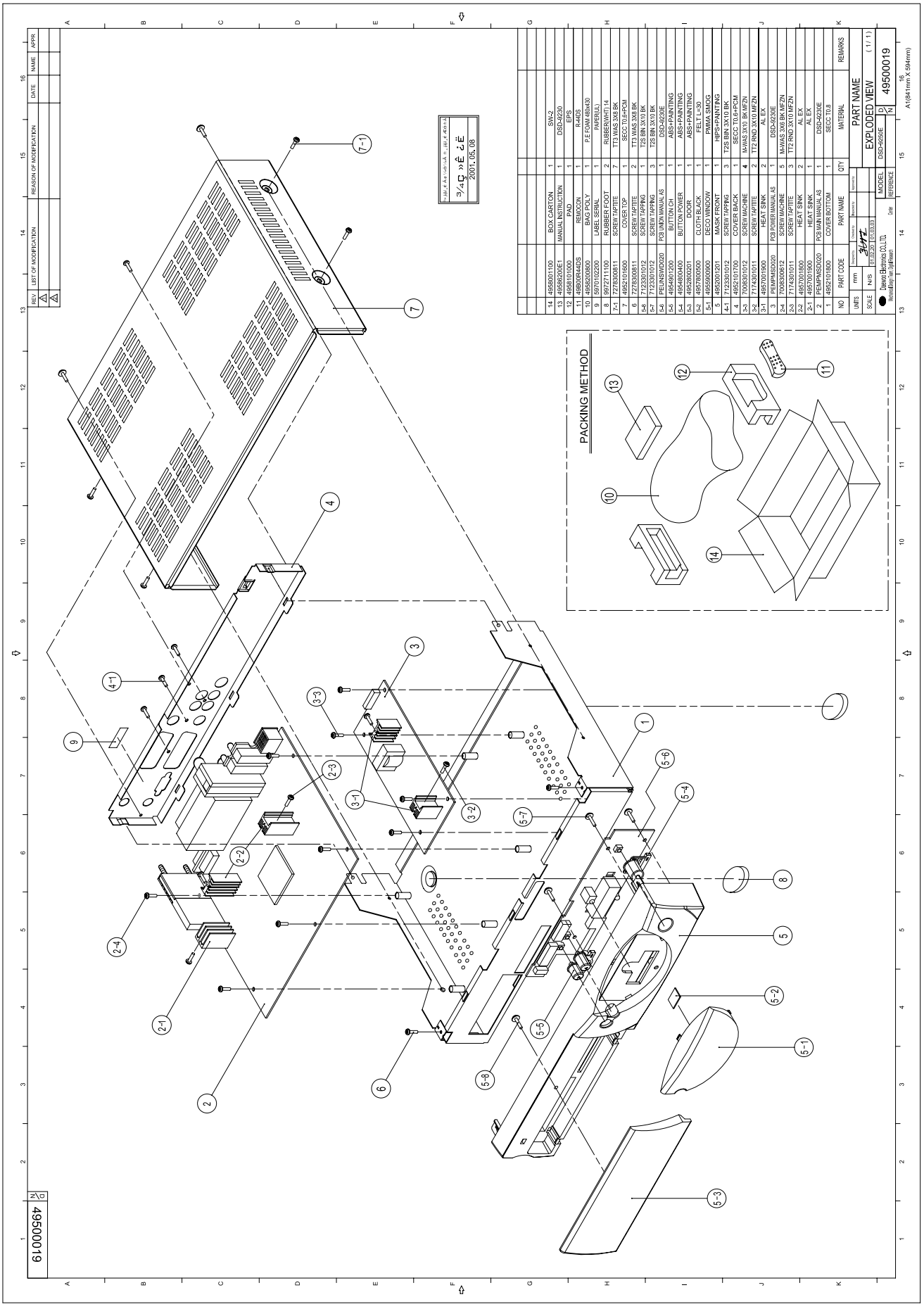
SCHEMATIC DIAGRAM



Ⅵ. PARTS PLACEMENT (ARRANGEMENT)

Ⅶ. PCB PATTERN

Ⅷ. EXPLODED VIEW



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